New Release

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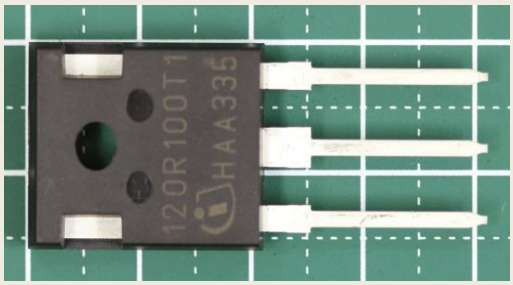
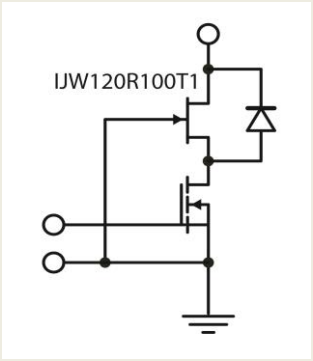
INFINEON IJW120R100T1 SIC POWER J-FET ANALYSIS REPORT

July 2017. LTEC Corporation released a detailed structure and process analysis report of the IJW120R100T1 1200V normally ON SiC J-FET power semiconductor device. This JFET is easily arranged in a cascode configuration using a low-voltage Si-FET device in order to realize a normally OFF configuration as shown below. The target applications are solar inverters, high voltage DC-DC, AC-DC converters, and bidirectional inverters.



Package

Die



Cascode configuration

Device features

- Max. operating voltage : 1200V, rated DC Drain current ID @25℃ = 26A
- Very low specific On-resistance, RON x A= 622mΩ x mm^2

The report has two individually purchasable sections: a Structure Analysis and a Process Analysis section. The Structure Analysis section reveals the physical construction of the device, including EDX materials analysis, and many other fine details. The Process Analysis section includes manufacturing process flow, the estimated number of photomasking steps, and the impurity concentration of the epitaxial layer.

Note: The listed report price may not be accurate as it decreases over time.
Please contact us for current report pricing : **info@ltecusa.com**

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