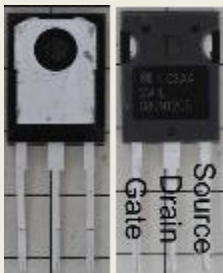


### ON SEMICONDUCTOR NVHL080N120SC1 AUTOMOTIVE CERTIFIED 1,200V SiC MOSFET SHORT CIRCUIT ROBUSTNESS ANALYSIS REPORT

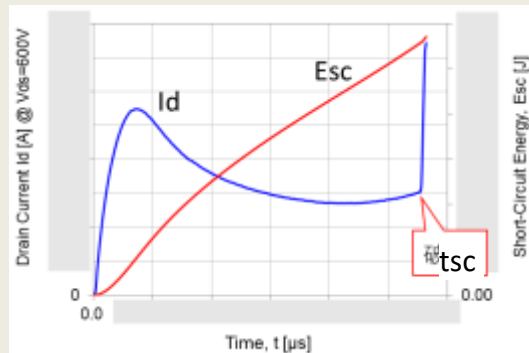
**February 2020.** The short-circuit (SC) capability of power transistors, especially SiC power MOSFETs, is one of the most critical reliability-related specifications. Compared to Si-based IGBTs, the size of the SiC transistor is smaller. This leads to significant reduction in SC endurance time ( $t_{sc}$ ).



Package



Die image



Drain current waveform and short-circuit energy (Esc)

#### Abstract

This is the first published short-circuit robustness analysis report that examines the correlation between short circuit robustness and the physical structure of the NVHL080N120SC1 device. This device is compliant with the AEC Q101 automotive standard.

#### The report includes:

- Identification of the mechanisms limiting short-circuit capability, measurements, physical analysis results, and extraction of the critical temperature ( $T_{j(crit)}$ ) at the onset of failure.
- Comparison of short-circuit robustness with other makers' 1,200V SiC MOSFETs. Examination of the differences in semiconductor structure, process, and their effect on short circuit robustness.
- Comparison of the electrical characteristics (off-state leakage current and temperature dependence) with other makers, and identification of differences and limitations.

#### Use value of the evaluation results in this report

- The minimum response time of the short-circuit protection circuit can be estimated.
- The internal device temperature can be estimated by performing electrothermal SPICE simulation using measured short-circuit drain current waveform and endurance time ( $t_{sc, f}$ ).

Note: The report price may change over time. For current price contact [info@ltecusa.com](mailto:info@ltecusa.com).

19G-0007-3

# Table of Contents

	Page
<b><u>Summary</u></b>	
Background, purpose and executive summary	3
<b><u>Physical analysis results</u></b>	
Device structure and material analysis	5
Table 1. Summary of each parameter	6
<b><u>Short circuit robustness evaluation</u></b>	
Evaluation circuit	7
Evaluation conditions	9
<b><u>Short circuit robustness evaluation results</u></b>	
Voltage and current waveforms	10
Table 3. Summary of measurement results	17
<b><u>Discussion for evaluation results</u></b>	
Peak drain current ( $I_{sc,pk}$ ) vs. drain voltage ( $V_{ds}$ )	19
Short circuit endurance time ( $t_{sc}$ ) vs. drain voltage ( $V_{ds}$ )	20
Short circuit energy ( $E_{sc,f}$ ) vs drain voltage ( $V_{ds}$ )	21
Short circuit endurance time( $t_{sc}$ ) vs power dissipation ( $P_d = I_d \times V_{ds}$ )	22
Gate leakage current considerations during SC	23
Estimation of junction temperature ( $\Delta T_j$ ) rise	27
Thermal impedance	30
<b><u>Comparison of transistor structure and electrical characteristics</u></b>	33
<b><u>Comparison of Onsemi's and Wolfspeed's 1,200V transistors</u></b>	
Electrical characteristic	35
Drain current at short circuit mode	37
<b><u>Conclusion</u></b>	39
<b><u>Appendix</u></b>	
References	40

# Excerpts from the report



Fig.2: Die

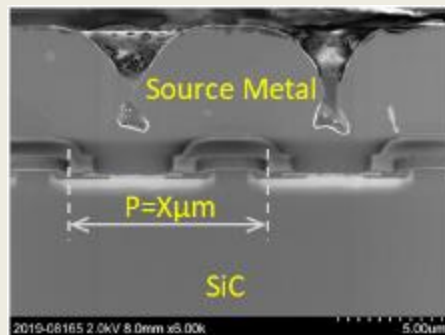


Fig.4: Cross-sectional image of SiC transistor

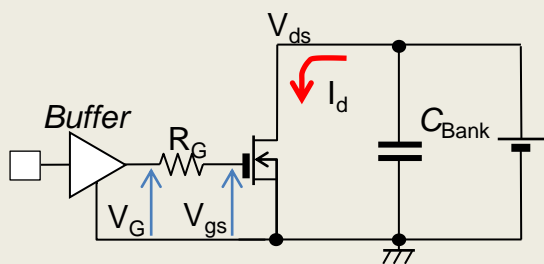


Table 2: Evaluation Conditions

#	V <sub>ds</sub> [V]	V <sub>gs</sub> [V]	Purpose
1	600	20	Basic SC characteristics
2	600	20	Check reproducibility
3	400	20	Drain voltage effect
4	800	20	“
5	600	16	Gate-Source voltage effect
6	600	24	“

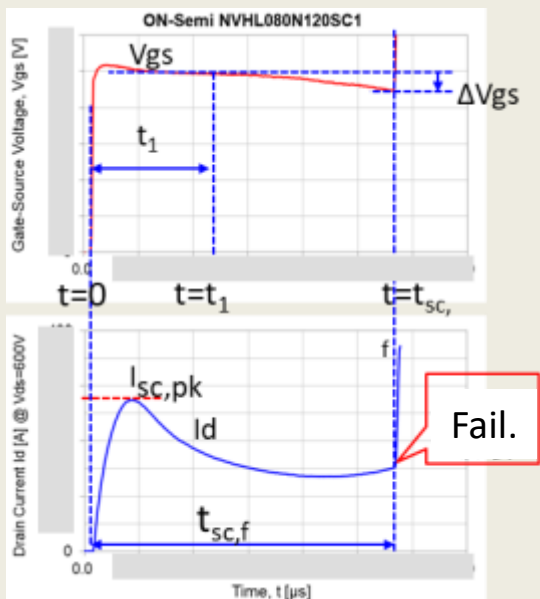


Fig.17: Measured gate-source voltage and drain current waveforms during SC event.

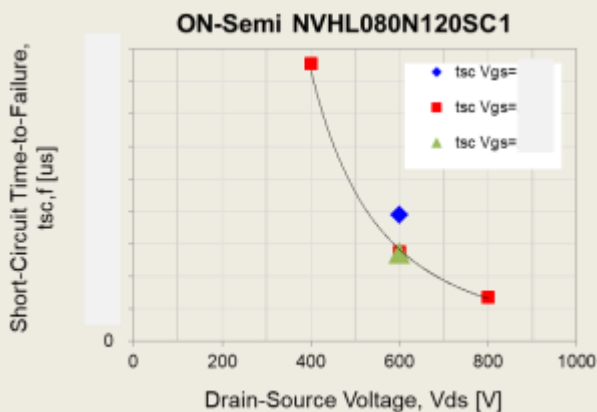
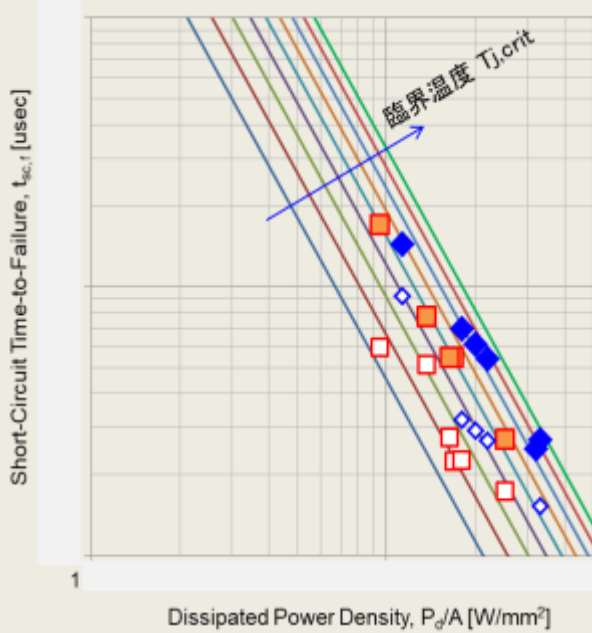
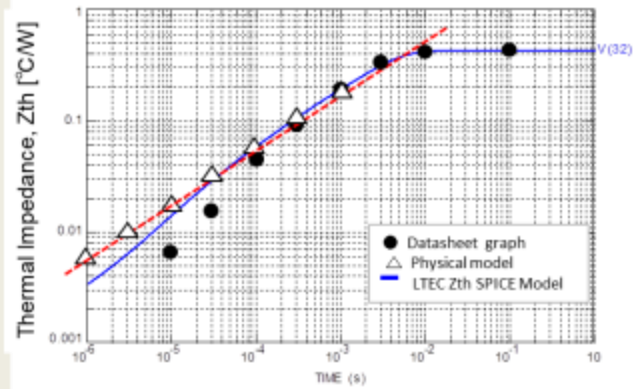


Fig.18: Measured dependence of the SC time to failure  $t_{sc,f}$  vs the drain voltage  $V_{ds}$ .

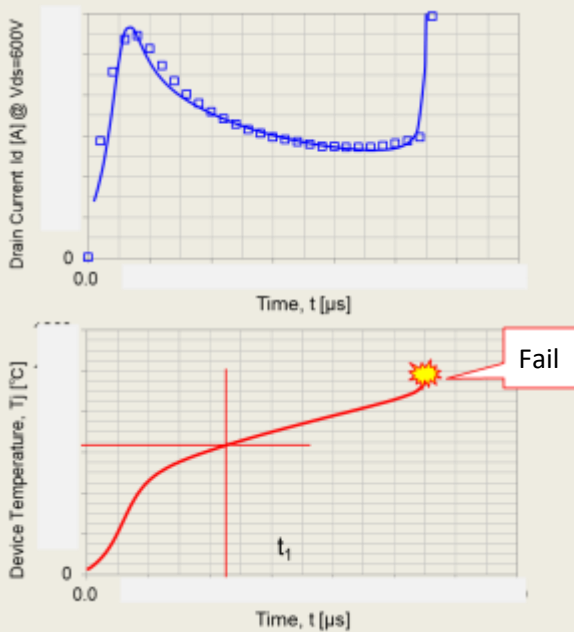
# Excerpts from the report (cont.)



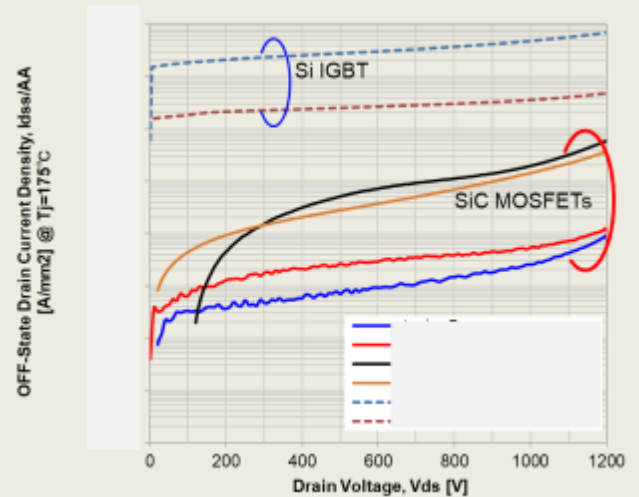
**Fig.28:** Measured short circuit durable time ( $t_{sc, f}$ ) vs. Power dissipation density  $P_d/A=(V_{ds} \times I_d)/A$ .



**Fig.29:** NVHL080N120SC1 Thermal impedance plot  
 ●: Data from datasheet,  
 (Blue line) Calculated using the SPICE model provided by manufacturer, and  
 (△) Calculated using the analysis result by LTEC



**Fig. 30:** Extracted transistor temperature rise using short circuit transient SPICE model



**Fig. 33:** Measured off-state drain current (@  $V_{gs} = 0V$ )