New Release

LTEC Corporation

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Infineon IMW120R045M1 CoolSiC MOSFET Extended Thermal Impedance SPICE Model

An extended thermal impedance model of the INFINEON CoolSiC transistor, applicable to describe short - circuit events with short power pulses (<100us), is provided. This thermal impedance model is based on device structure and material analysis, and numerical simulation.

Background

The short-circuit event is characterized by high current high power pulses of less than 10us where the internal temperature of the transistor rises above the normal operating range (Tjmax ~ 175°C). We experimentally verified that the short-circuit failure of the INFINEON CoolSiC transistor was caused by the melting of the Al source electrode material, causing a short circuit between the gate and source electrodes (*).

Based on Zth and short-circuit pulse power measurement results described in the manufacturer's data sheet, the device temperature at the time of failure is estimated to be 200 to 300°C. However, this estimation using the data sheet Zth is not valid, since it does not agree with the observed result of Al melting (Tm≅660°C).

[*] Analysis result by LTEC. Contact LTEC Corporation for a released short-circuit withstand capability evaluation report of this product.

LTEC extended thermal impedance model

Based on the above observations, we analyze the device structure, physically simulate the heat flow, and synthesize the thermal impedance Zth at the time of failure. With this approach, the effective thermal equivalent circuit model for short-circuit conditions can be extended to the microsecond range.

Features and application of the extended Zth model

- The extracted Zth model is based on a physical mechanism.
- The Zth model is synthesized taking into account the time to short-circuit fault (tsc) obtained by measurement and the drain current waveform.
- Provides a thermal equivalent circuit compatible with SPICE.

Report Content:

- Problem description of thermal impedance Zth data of power MOSFET devices
- Device structure / material analysis
- Thermal simulation analysis
- Thermal equivalent circuit (synthesis with Cauer Model)
- SPICE model and thermal simulation results

※If you already purchased the IMW120R045M1 short-circuit withstand capability evaluation report, the price of this report is $3,000.

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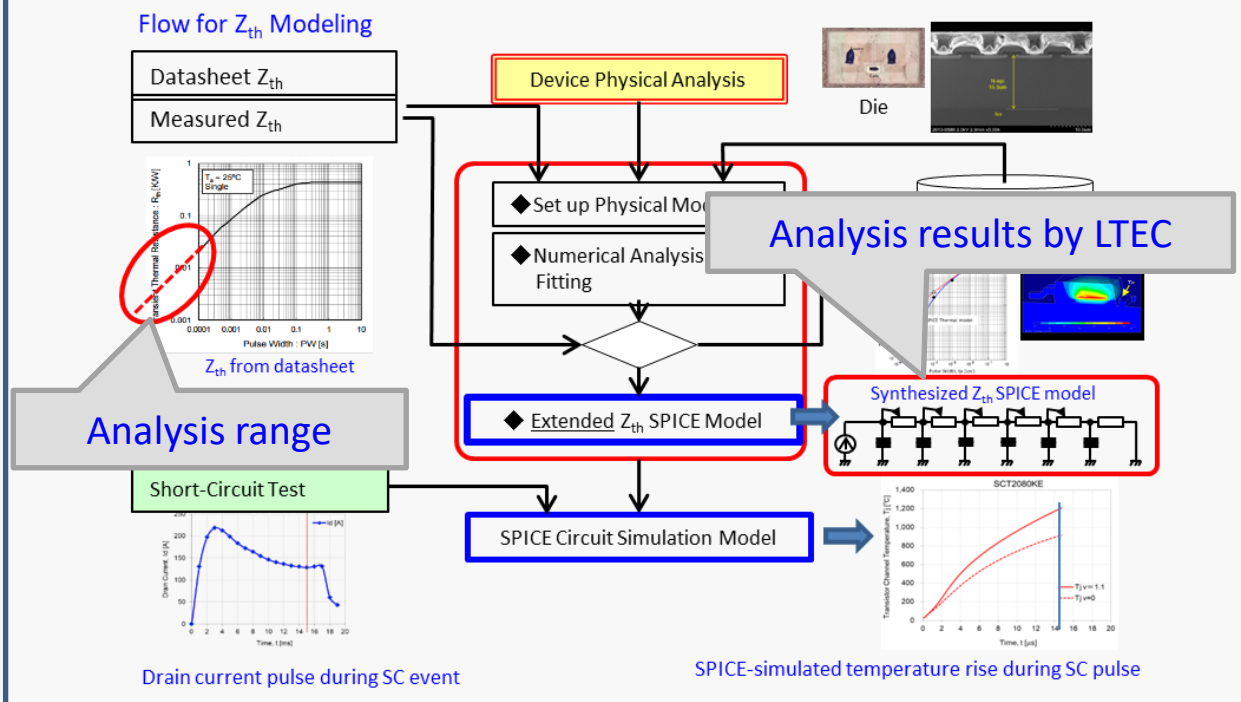
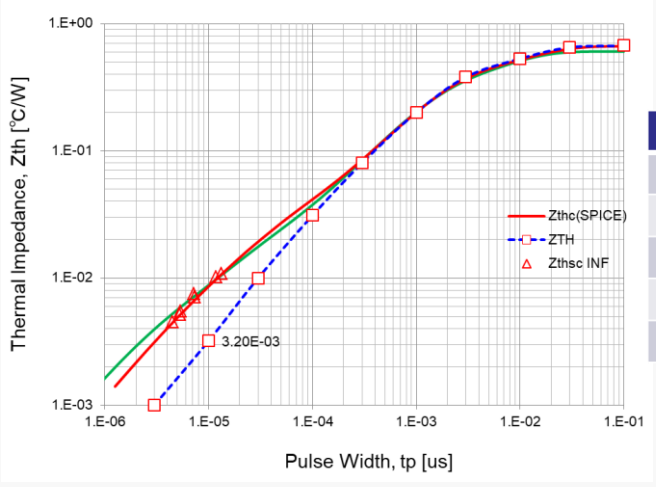


Fig.1: Method applied for extracting thermal impedance for short ON-time pulses in power transistors.



Rck	°C/W	Cck	W·sec/°C
Rc1	0.	Cc1	0
Rc2	0.	Cc2	0
Rc3	0.	Cc3	0
Rc4	0.	Cc4	2
Rc5	0.	Cc5	5

Table 1: Synthesized Cauer thermal equivalent circuit SPICE model parameters

Fig.2: Graph of thermal impedance Zth as a function of on-time pulse width tp.
Zth from the manufacturer's data sheet (□) and SPICE model (blue line). Zthsc (△) compiled from short-circuit tests , LTEC structural analysis simulation (green line), and synthesized SPICE model (red line).

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