

# Improve New Product Positioning, Reduce Time to Market, Protect Your IP Through Benchmarking and Deep Analysis

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LTEC Corporation

member

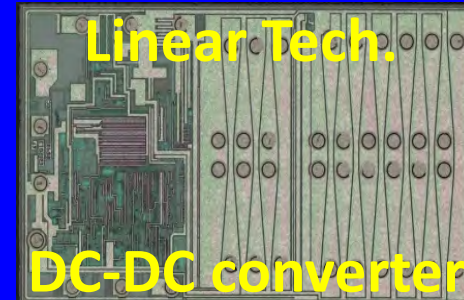
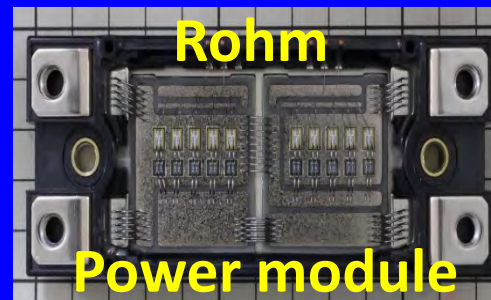
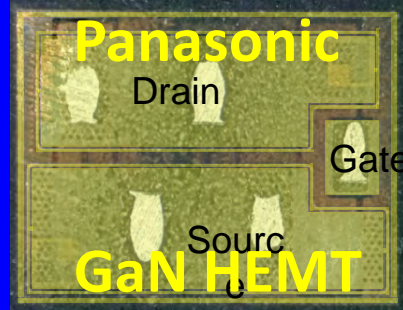
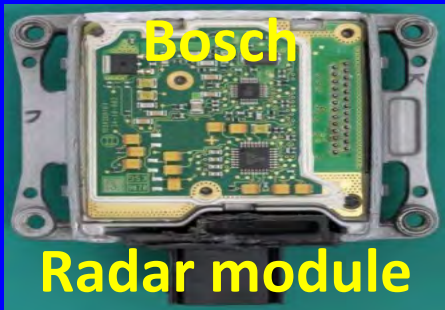
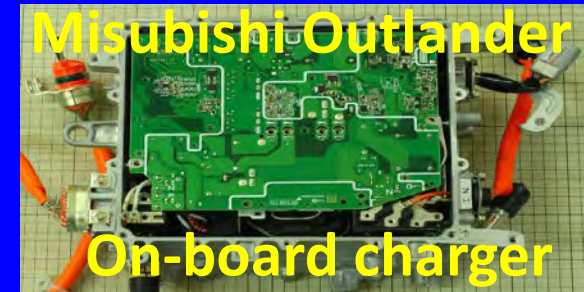
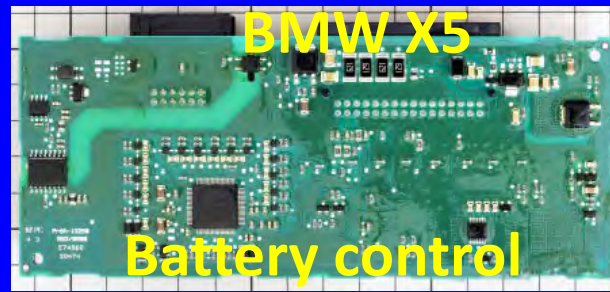
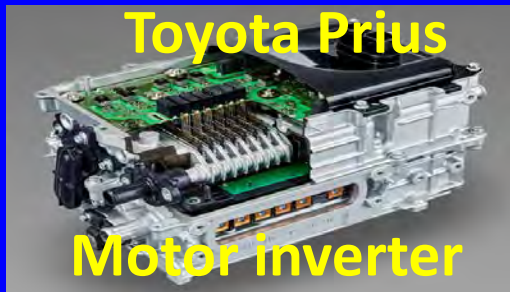


# Introduction

- ❑ About LTEC corporation
- ❑ Definition of terms:
  - ❑ Technical Analysis (Hardware, IP)
  - ❑ Reverse Engineering (RE)
- ➔ ❑ Re-inventing RE: Harvesting the synergies between product development and learning through RE:
  - ❑ Collaborative RE (CRE)
  - ➔ ❑ Collaborative Outsourced RE (CORE)
- ➔ ❑ Practical (real life) examples
- ❑ Summary

# About LTEC Corporation

- ❑ LTEC is Japan's dominant provider of intellectual property services. We provide
  - ❑ Technical analysis of products released to market
  - ❑ Intellectual property (patents) analysis
  - ❑ Technology analysis



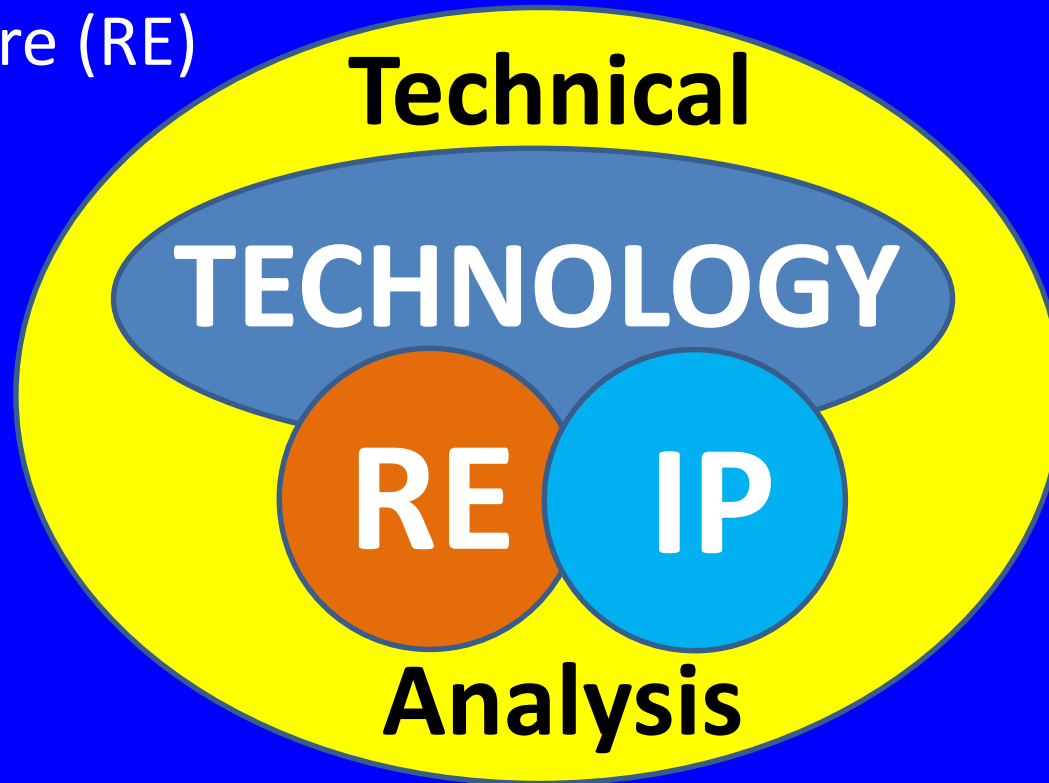
# LTEC Corporation and Its Client Base

Region	Companies
Japanese Electrical manufacturers Semiconductor/Component manufacturers	Panasonic, Toshiba, SONY, NEC, Hitachi, Mitsubishi, Murata, Taiyo Yuden, Rohm, Renesas, TDK, Sharp (Foxconn), Yamaha
Japanese Automotive manufacturers	Toyota, Mitsubishi motors, Mazuda, Denso, Aishin, Hitachi automotive, Yazaki, Calsonickansei, Yamaha
USA Semiconductor manufacturer	Qualcomm, On-Semiconductor, IDT, Maxim, Intel (Altera),
Korean Automotive manufacturer	Hyundai automotive, LGE
Korean Electrical manufacturer	Samsung, LGE
Taiwanese Semiconductor manufacturer	MediaTek, TSMC

# Definition of Terms

# Technical Analysis - Definition

- ❑ Focused **secondary research** involving
  - ❑ Intellectual property (IP), patents
  - ❑ Technology
  - ❑ Hardware: Reverse Engineering (RE)
  - ❑ Software (RE)



# Reverse Engineering (RE) - Definition

- ❑ RE is process to extract knowledge or design blueprints from anything man made.
- ❑ RE is about **learning** about new technologies, know-how not yet available from textbooks, patents and other publications just yet; about latest technologies.
- ❑ RE teaches you things not readily available.
- ❑ RE helps your company to remain competitive.



*I have a lot more to  
say about this!*

*Come to Booth 1339*

# Example



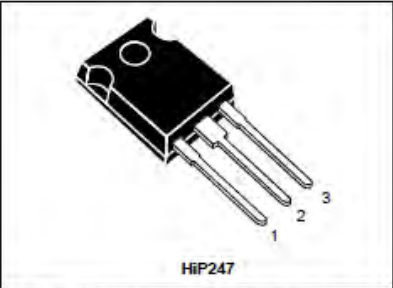
# Example: Learning through RE

Example: RE performed on latest generation SiC MOSFETs. How is  $T_j=200^\circ\text{C}$  operation achieved by new package EMC?

**SCT30N120**

Silicon carbide Power MOSFET 1200 V, 45 A, 90 mΩ  
(typ.,  $T_j = 150^\circ\text{C}$ ) in an HiP247™ package

Datasheet - production data



HiP247

**Features**

- Very tight variation of on-resistance vs. temperature
- Very high operating temperature capability ( $T_j = 200^\circ\text{C}$ )**
- Very fast and robust intrinsic body diode
- Low capacitance

**Applications**

- Solar inverters, UPS
- Motor drives
- High voltage DC-DC converters

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	1200	V
$V_{GS}$	Gate-source voltage	-10 to 25	V
$I_D$	Drain current (continuous) at $T_c = 25^\circ\text{C}$ (limited by die)	45	A
$I_D$	Drain current (continuous) at $T_c = 25^\circ\text{C}$ (limited by package)	40	A
$I_D$	Drain current (continuous) at $T_c = 100^\circ\text{C}$	34	A
$I_{DM}^{(1)}$	Drain current (pulsed)	90	A
$P_{TOT}$	Total dissipation at $T_c = 25^\circ\text{C}$	270	W
$T_{stg}$	Storage temperature range	-55 to 200	$^\circ\text{C}$
$T_j$	Operating junction temperature range		$^\circ\text{C}$

**SCH2080KE**  
N-channel SiC power MOSFET co-packaged with SiC-SBD

Data Sheet

$V_{DSS}$	1200V
$R_{DS(on)}$ (Typ.)	80mΩ
$I_D$	40A
$P_D$	262W


**Features**

- Low on-resistance
- Fast switching speed
- Fast reverse recovery
- Low  $V_{SD}$
- Easy to parallel
- Simple to drive
- Pb-free lead plating ; RoHS compliant

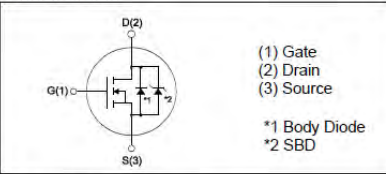
**Absolute maximum ratings ( $T_a = 25^\circ\text{C}$ )**

Parameter	Symbol	Value	Unit
Drain - Source voltage	$V_{DSS}$	1200	V
Continuous drain current	$T_c = 25^\circ\text{C}$	$I_D^{*1}$	40
	$T_c = 100^\circ\text{C}$	$I_D^{*1}$	28
Pulsed drain current	$I_{D,pulse}^{*2}$	80	A
Gate - Source voltage (DC)	$V_{GSS}$	-6 to 22	V
Gate - Source surge voltage ( $T_{surge} < 300\text{nsec}$ )	$V_{GSS,surge}^{*3}$	-10 to 26	V
Power dissipation ( $T_c = 25^\circ\text{C}$ )	$P_D$	262	W
Junction temperature	$T_j$	175	$^\circ\text{C}$
Range of storage temperature	$T_{stg}$	-55 to +175	$^\circ\text{C}$

**Outline**  
TO-247



**Inner circuit**



(1) Gate  
(2) Drain  
(3) Source  
\*1 Body Diode  
\*2 SBD

**Packaging specifications**

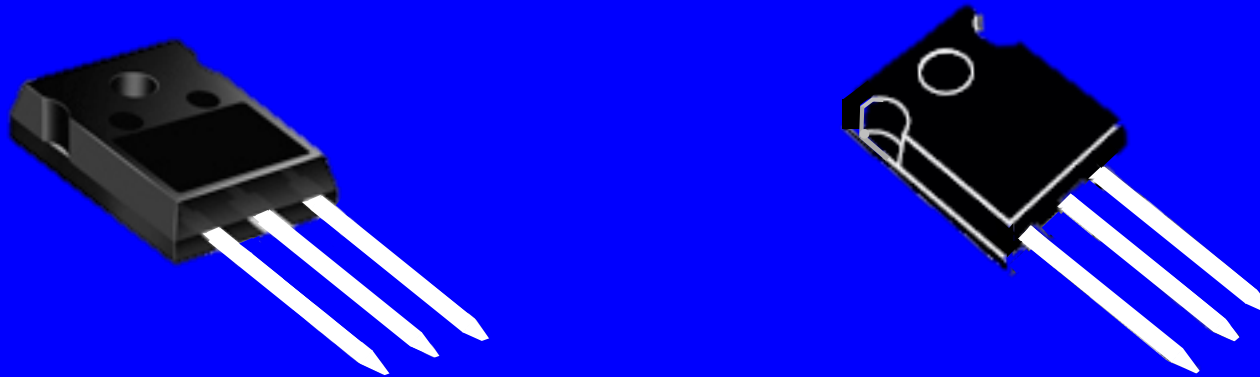
Packing	Tube

# Learning through RE

- Example: We performed RE on latest generation SiC MOSFETs.

How is  $T_j=200^\circ\text{C}$  operation achieved by new package EMC?

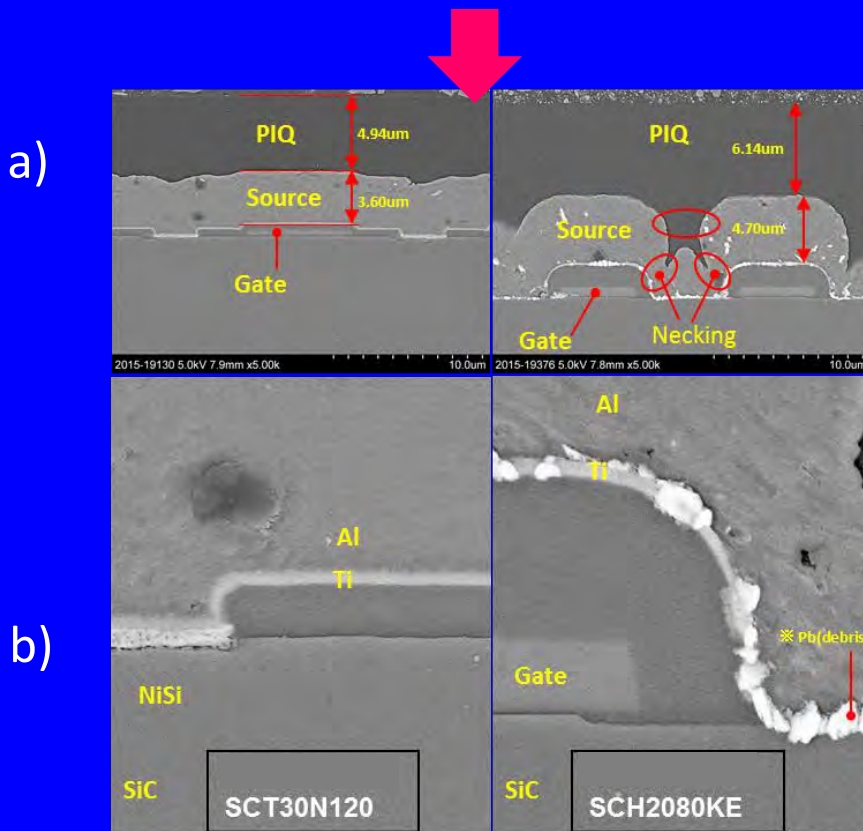
$T_j=200^\circ\text{C}$  Continuous  $\longleftrightarrow$   $T_j=150^\circ\text{C}$  Abs. Max.  
 $T_{\text{storage}}=200^\circ\text{C}$



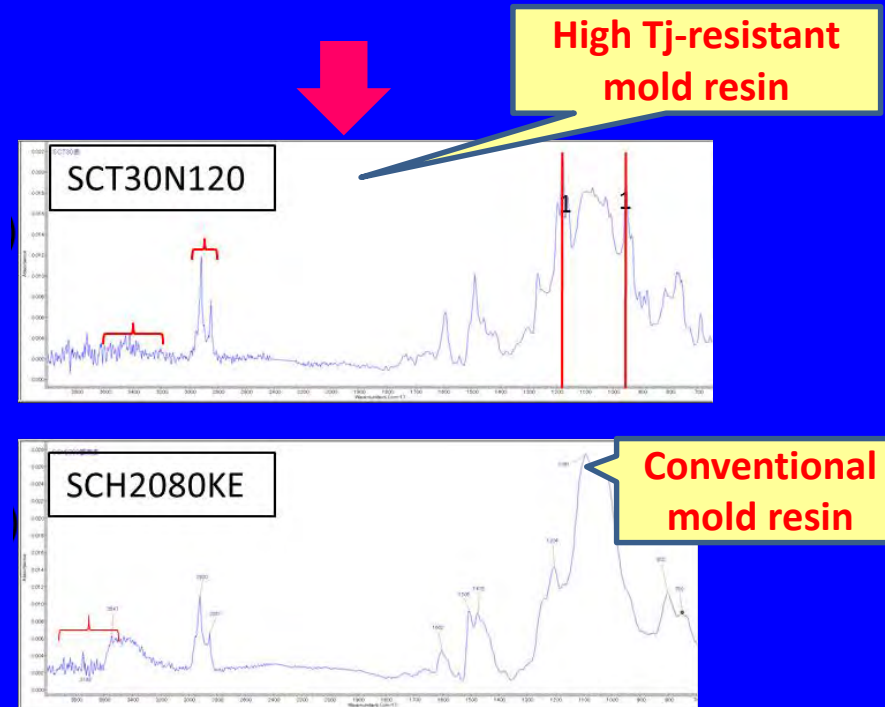
**➔ What are the key enablers?**

# Enabling Continuous 200°C Operation

## □ Evidence:



SEM cross-section observation of evaluated SiC devices. (a) Transistor structure. (b) Detail of the top metal (source) electrode.



Measured package resin FTIR spectrum of samples (a) SCT30N120 (SiC T<sub>j</sub>max = 200°C), and b) the SCH2080KE (SiC T<sub>j</sub>max = 175°C). Strong peaks (around 980 cm<sup>-1</sup> and 1200 cm<sup>-1</sup>) in the SCT30N120 SiC device package are observed.

# RE vs. IP Analysis: Different Objectives, Identical Methodology

**R&D AND PRODUCT  
DEVELOPMENT DEPARTMENTS**

**IP (PATENT) DEPARTMENTS  
AND LAW FIRMS**

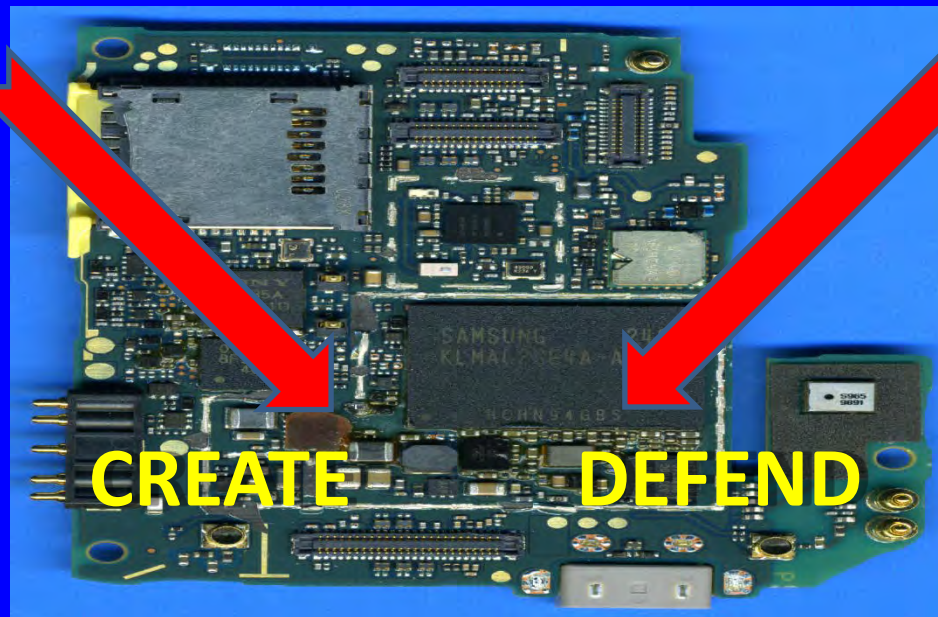
**WANTS TO KNOW:  
COMPETITORS' PRODUCTS  
AND TECHNOLOGIES**



**WANTS TO KNOW:  
COMPETITORS' IP AND  
TECHNOLOGIES**



**ANALYZE  
LEARN  
UNDERSTAND**



**ANALYZE  
LEARN  
UNDERSTAND**

**CREATE**

**DEFEND**

# Our Unique Approach to RE

# Re-inventing RE

- ❑ About LTEC corporation
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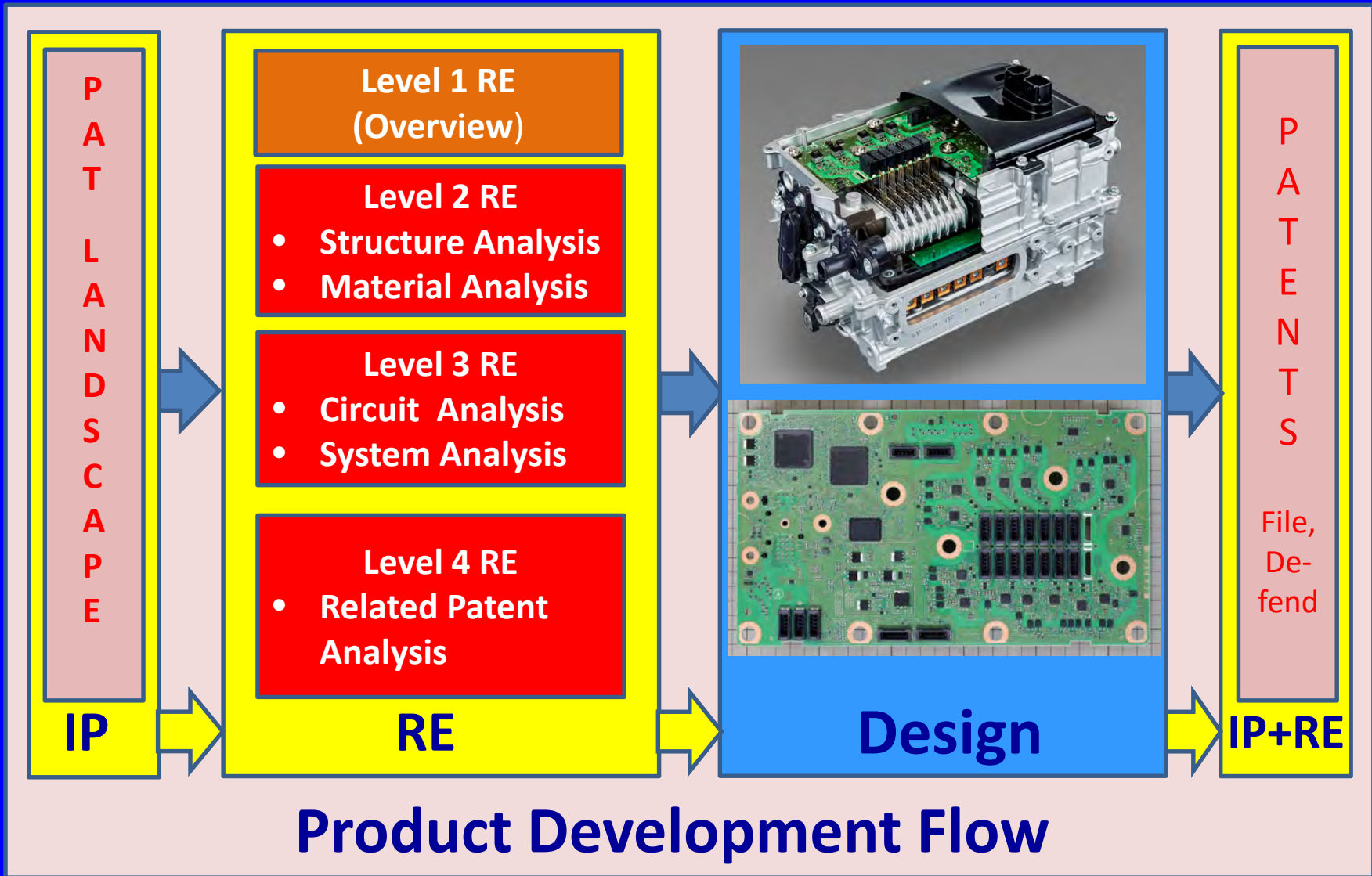
# A Unique Approach to Technical Analysis

## Collaborative Reverse Engineering (CRE)

## Collaborative Outsourced Reverse Engineering (CORE)

- ❑ Provides dynamically targeted RE by working collaboratively and interactively with
  - ❑ Product development teams
  - ❑ IP analysis and protection teams
- ❑ Facilitates fast learning through RE in a way that
  - ❑ Enhances new product positioning
  - ❑ Accelerates the pace of product development

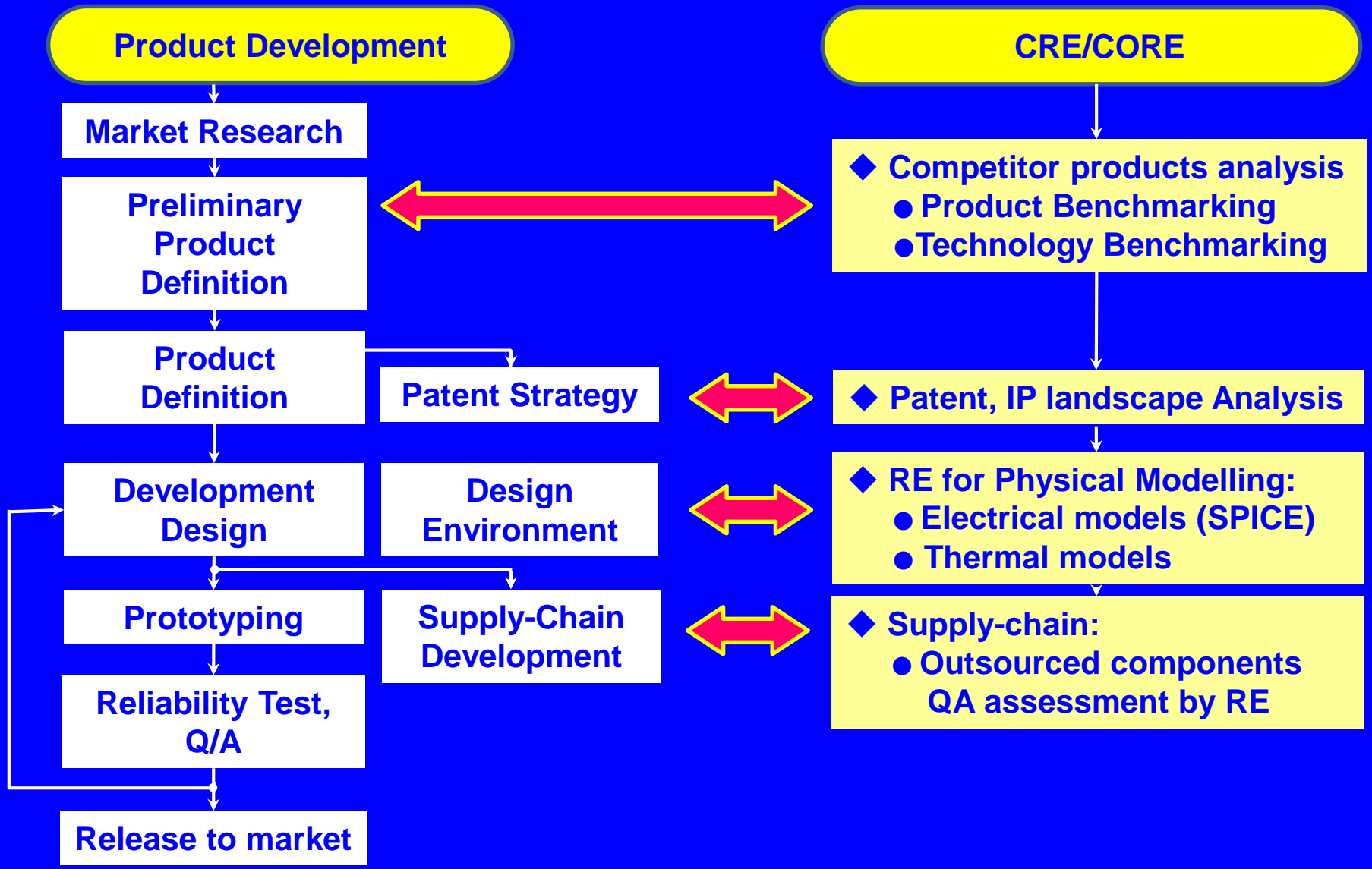
# RE in Product Development



*Recognize: RE is a natural starting point to develop creative new ideas*



# CORE Provides Active Support in Product Development



# Why “Collaborative” RE?

- ❑ Manpower/resource utilization
  - ❑ Enhanced productivity → faster time to market
  - ❑ Parallel vs. serial process → faster time to market
  - ❑ Unique know-how
  - ❑ Cost of labor
- ❑ Delivers deep understanding of your competitors’ strengths and weaknesses prior to product definition
  - more competitive product
  - ❑ Uncovers hidden features, materials, trends
  - ❑ Helps avoid re-inventing the wheel
- ❑ Mitigates risks

# Why “Outsourced”?

- ❑ You can
  - ❑ free up designers to focus on product development
    - ➔ faster time to market!
  - ❑ build a solid foundation for design activity by benefiting from our
    - ❑ broad knowledge gained from analyzing similar products
    - ❑ knowledge of the latest technology
    - ❑ proprietary tools and methodologies

# Examples

# Example: Why “Outsource”?

- ❑ Understand your competition (hardware, software, and patents, technology) prior to product definition/design



Performance?

Reparability?



Features?

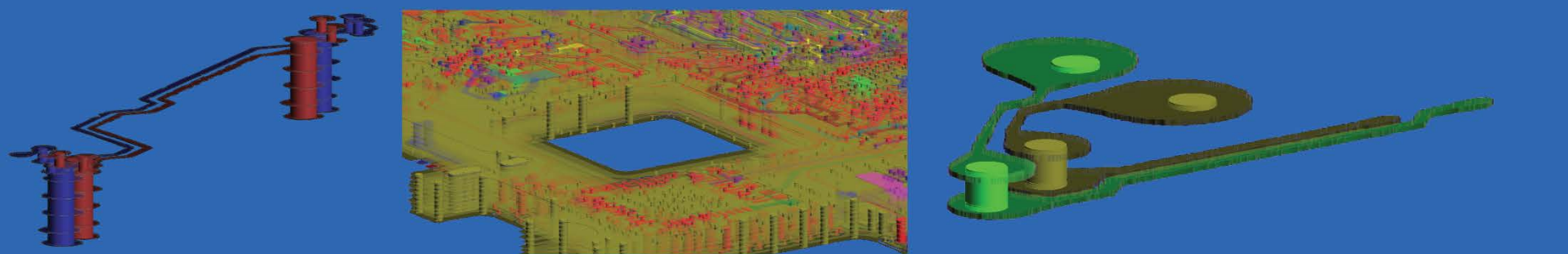
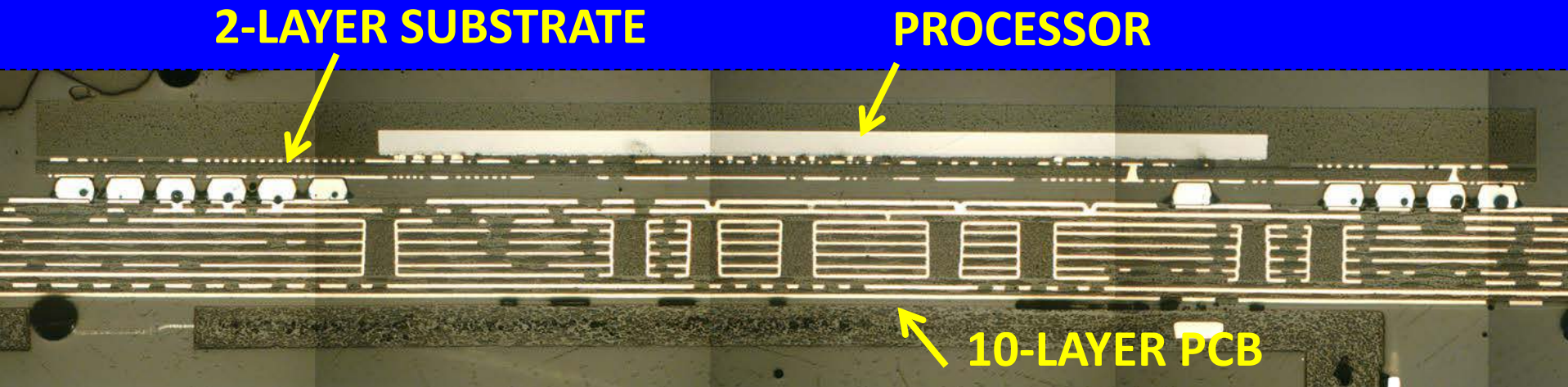
Design improvements?



***Learn from the past, learn from the best, apply to the future***

# Example: Collaboration with Design Teams

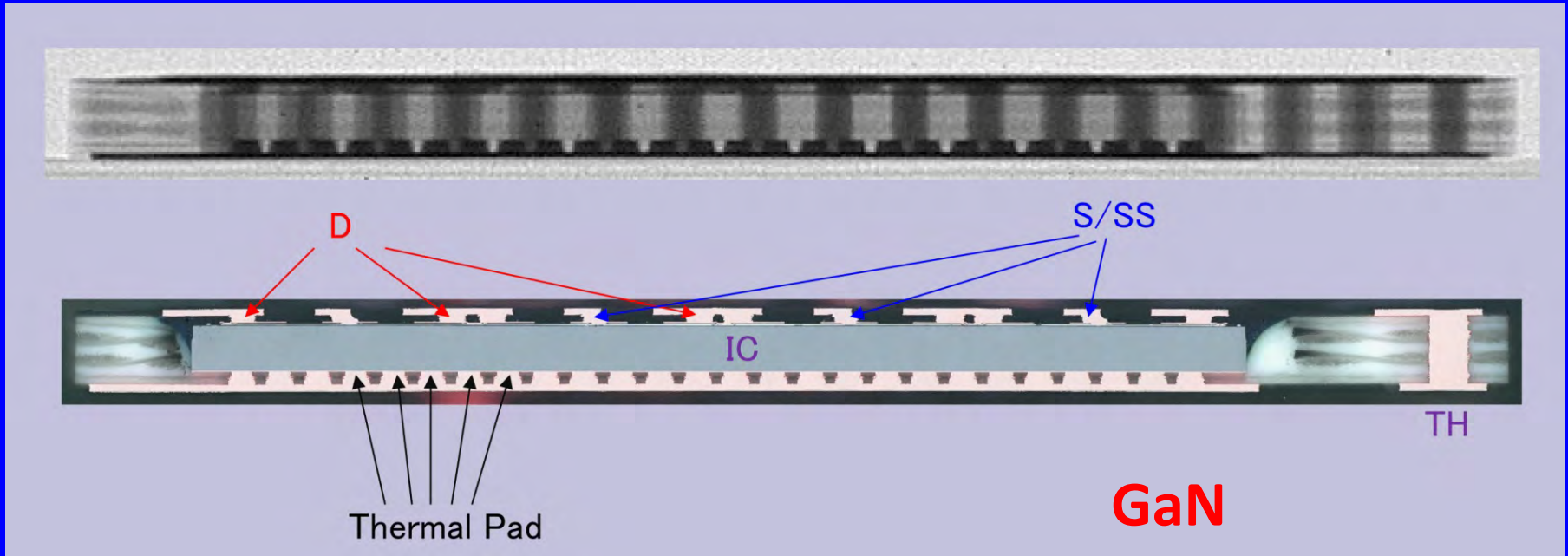
- ❑ Is manpower available to do the work in-house?
  - ❑ RE is labor intensive!
  - ❑ Parallel RE and design vs. serial? Faster time to market!



**3D model for EM field solver (PDN analysis)**

*3D model for PDN or signal integrity analysis in compatible file format*

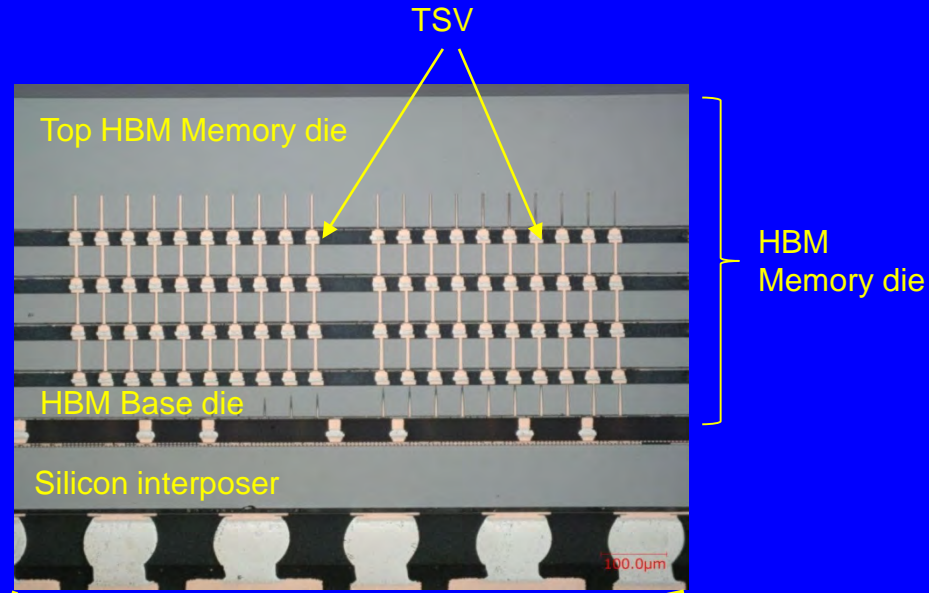
# Example: Understand Latest Technology



# Example: Understand Latest Technology

AMD (Radeon R9 Fury X)

**Interconnect Technology in 3D packaging is a major challenge!**



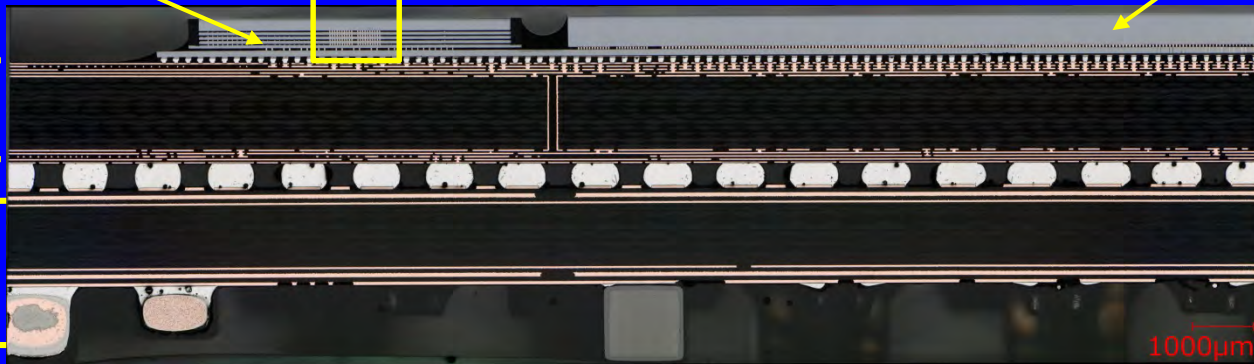
Stacked High Band Memory (HBM)

Processor (CPU, GPU)

Silicon interposer

Package substrate

PCB





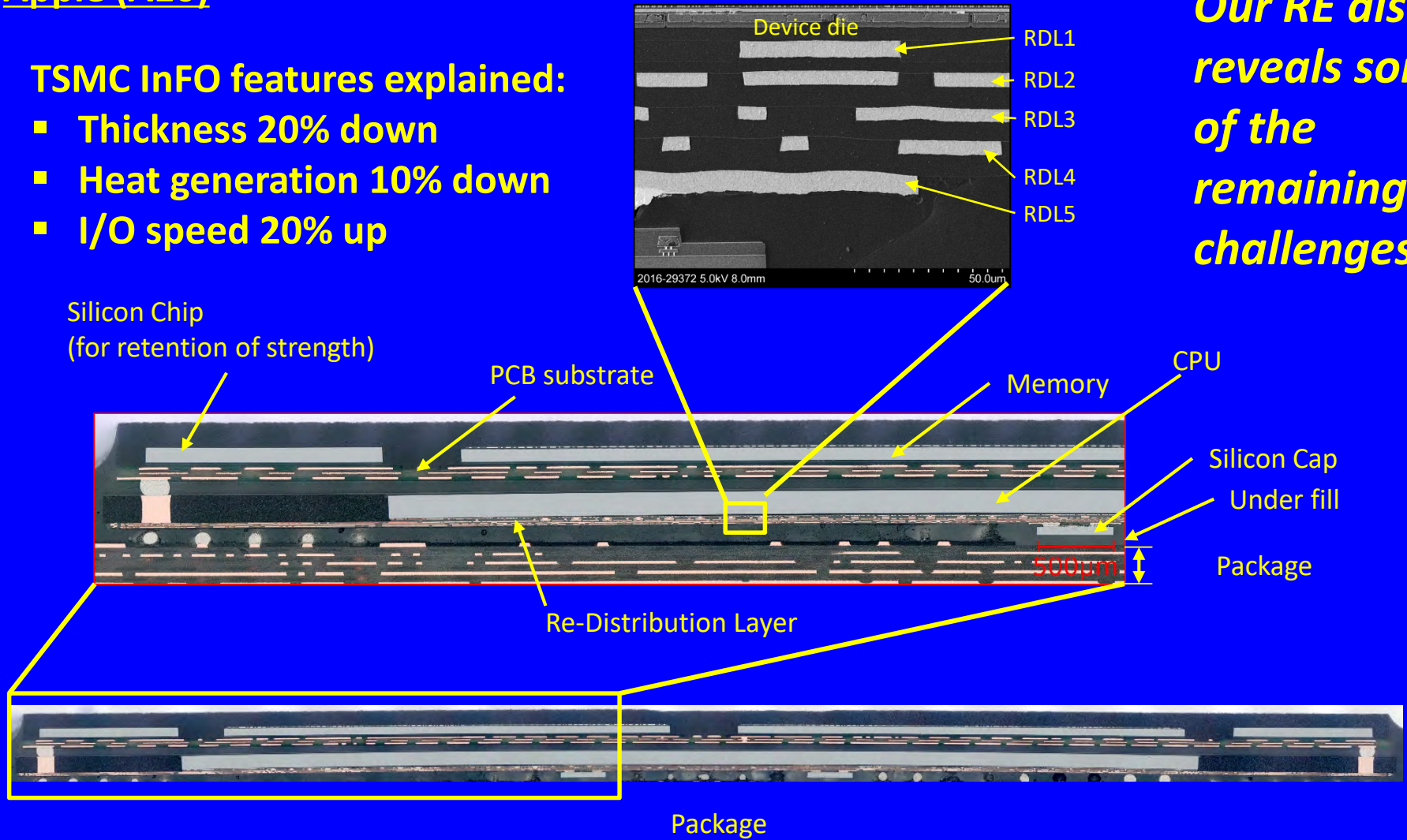
# Example: Understand Latest Technology

## Apple (A10)

### TSMC InFO features explained:

- Thickness 20% down
- Heat generation 10% down
- I/O speed 20% up

*Our RE also reveals some of the remaining challenges!*



# Example: Finding the Not So Obvious...

- RE reveals essential features, materials not shown in the datasheet, nor discussed in conferences!

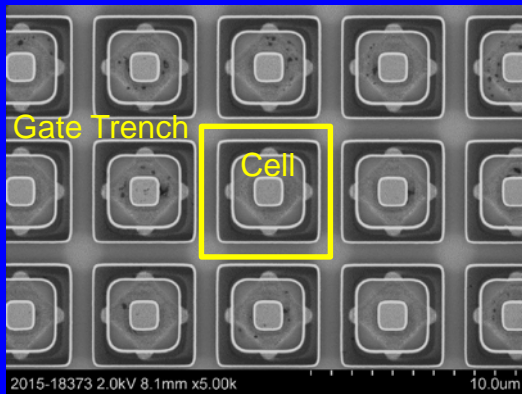
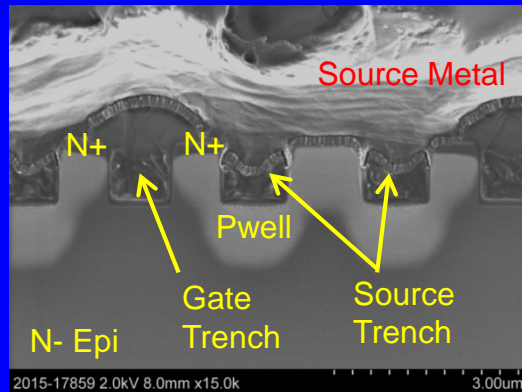
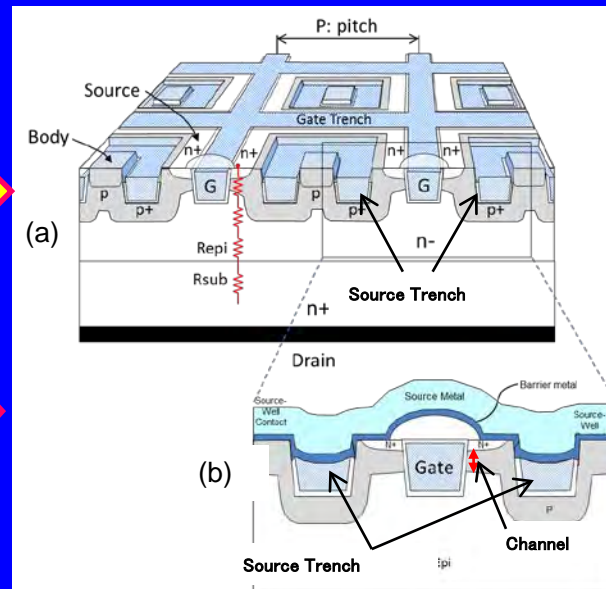


Fig.1-1: SiC MOSFET cell array



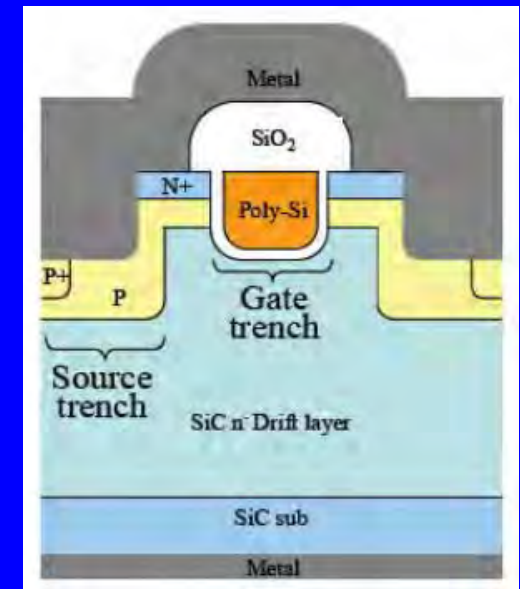
SiC MOSFET cross-section

This is what we give you



Reconstructed details

This is what you get

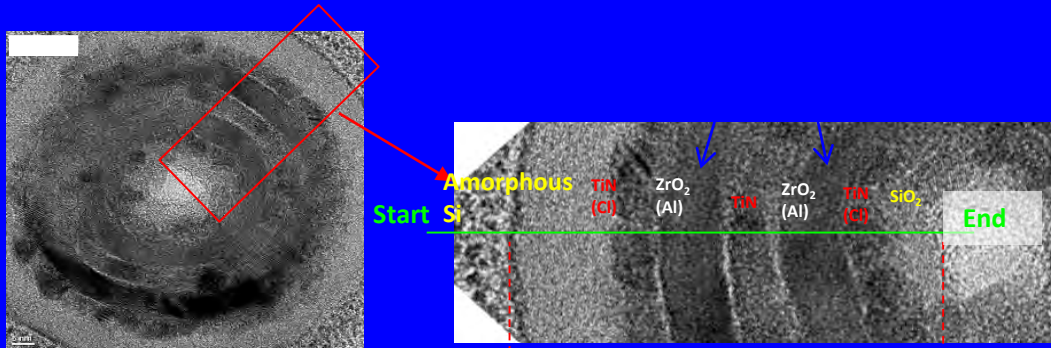


Essential details not shown or published anywhere

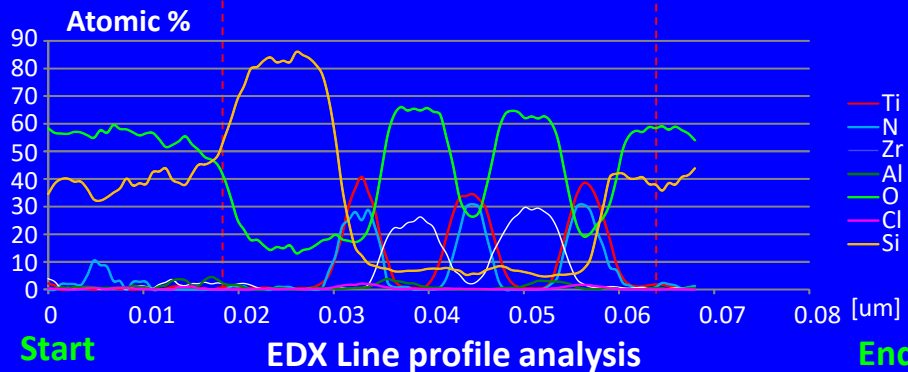
# Example: Deep Analysis

Image sensor material analysis: find ultra-low volume of Al within ZrO<sub>2</sub> layer within an

- Measure the characteristic X-ray energy
- Convert to atomic %
- Characteristic X-ray has specific energy of element by element



Quantitative analysis

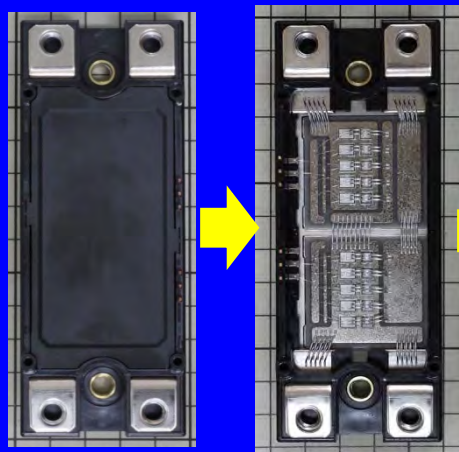


Atom-%

- ① Si:74.17% O:17.99%
- ② Ti:29.84% N:23.95% O:23.66%  
Cl:1.70%
- ③ Zr:21.48% O:62.88% Al:1.82%
- ④ Ti:30.35% N:22.31% O:34.73%
- ⑤ Zr:24.55% O:59.82% Al:1.89%
- ⑥ Ti:30.71% N:22.55% O:24.96%  
Cl:1.25%
- ⑦ Si:39.61% O:54.71%

# Example: RE-based Physical Modeling

□ Ex.: RE analysis and thermal model of SiC power module

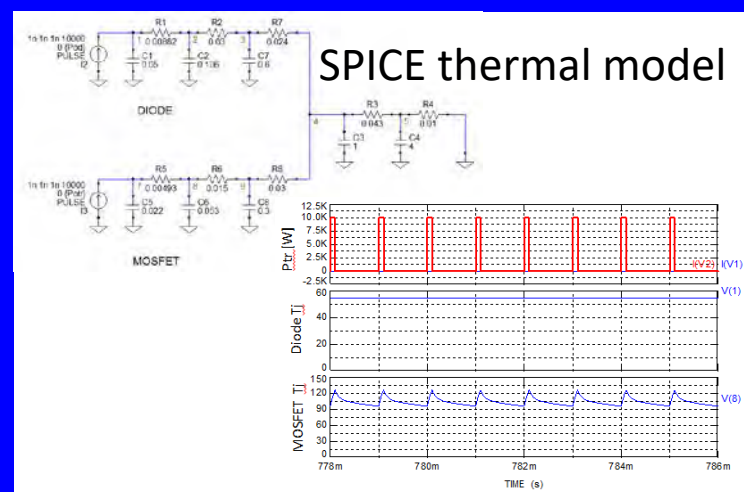
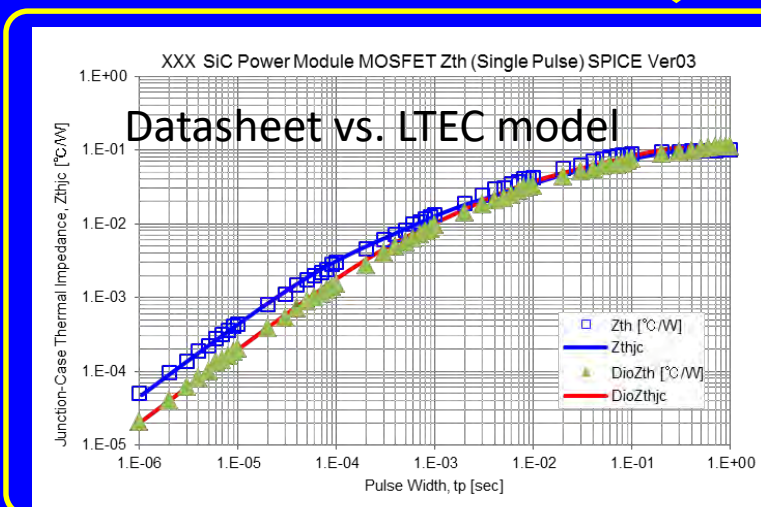


SiC Power Module

**Die attach**  
Detected elements :  
Sn,Sb,Ag,Cu,Ni

**Power module physical and materials analysis through RE**

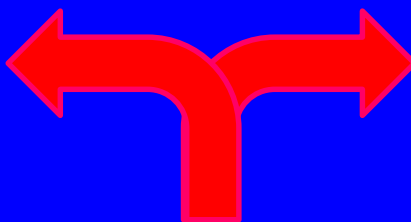
Electro-thermal model



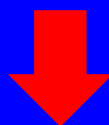
# Example: Avoid Re-inventing the Wheel



59% 41%



- ❑ A USPTO study found that  
“For the patents where at least one claim was held *unpatentable*, the prior art used by PTAB had been in front of the examiner during prosecution *59 percent of the time.*” Source: USPTO, Jan. 2015



# Tools of Our Trade

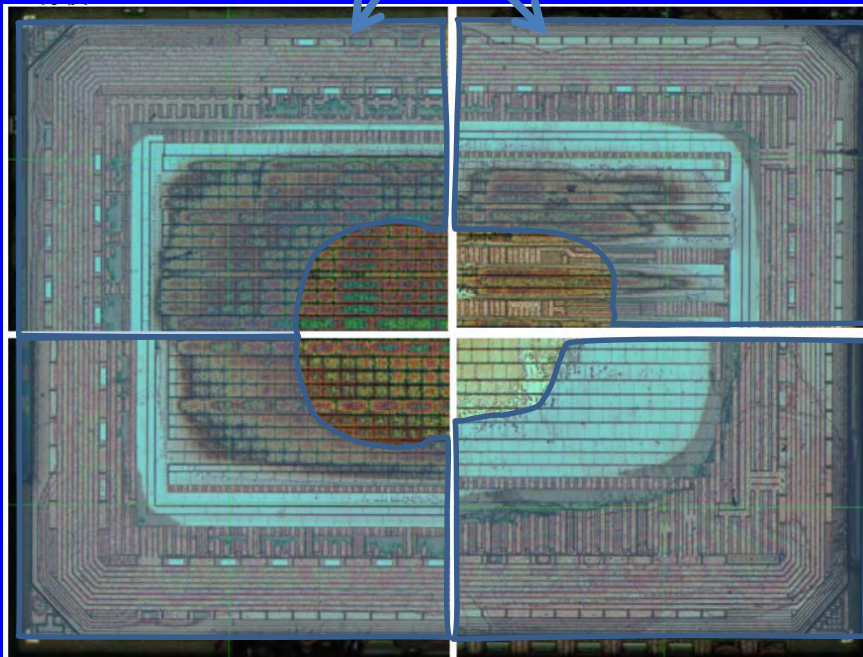
# Advanced Productivity Enhancement and Modeling Tools

# The **Art** of Delayering

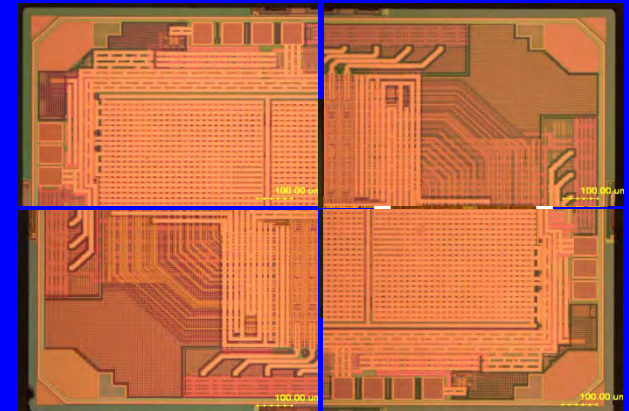
Fatal over-polishing may occur in the die peripheral portion can be easily predicted.



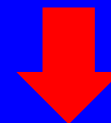
Over-polished region



Typical over-polishing



Proprietary delayering  
Technology down to 10nm

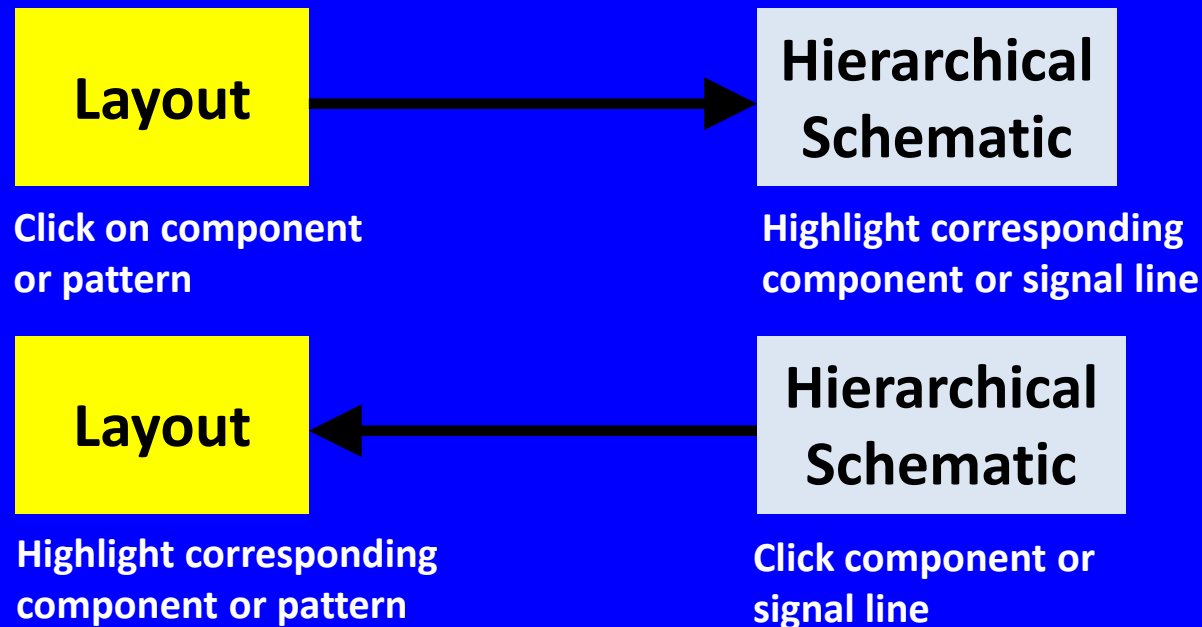




# Enhancing **Productivity**: PCB Schematic Viewer

Facilitates cross-probing between

- ❑ schematic diagram and components in the PCB, or
- ❑ schematic diagram and components in the reconstructed layout images



# Advanced Schematic Viewer

1. Click the signal line in the layout viewer

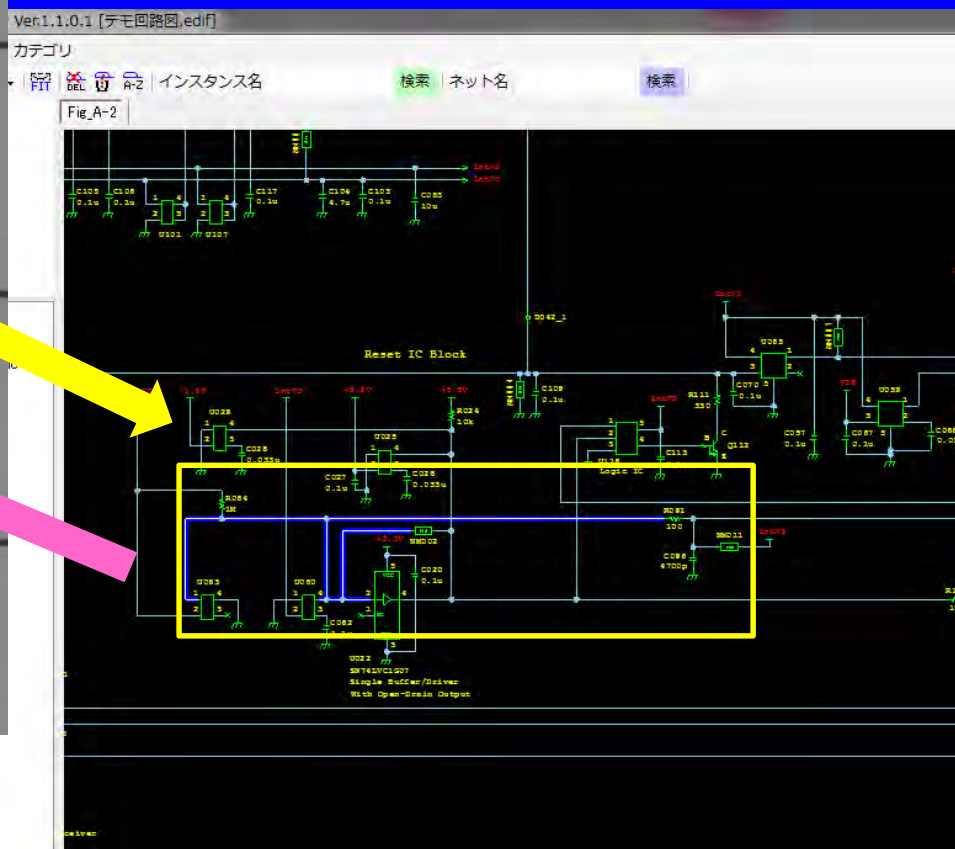
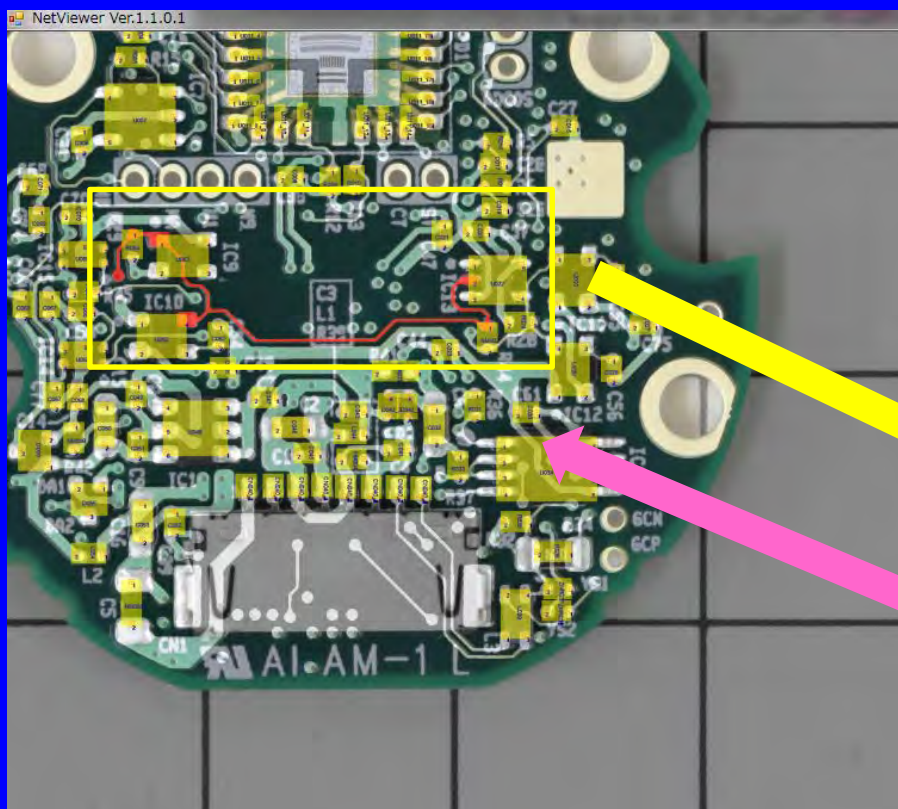


2. Highlight the corresponding signal line in the circuit viewer

2. Highlight the corresponding signal line in the layout viewer



1. Click the signal line in the schematic viewer



# Advanced Schematic Viewer

1. Click the component in the layout viewer



2. Highlight the corresponding component in the schematic viewer

2. Highlight the corresponding component in the layout viewer



1. Click the component in the schematic viewer

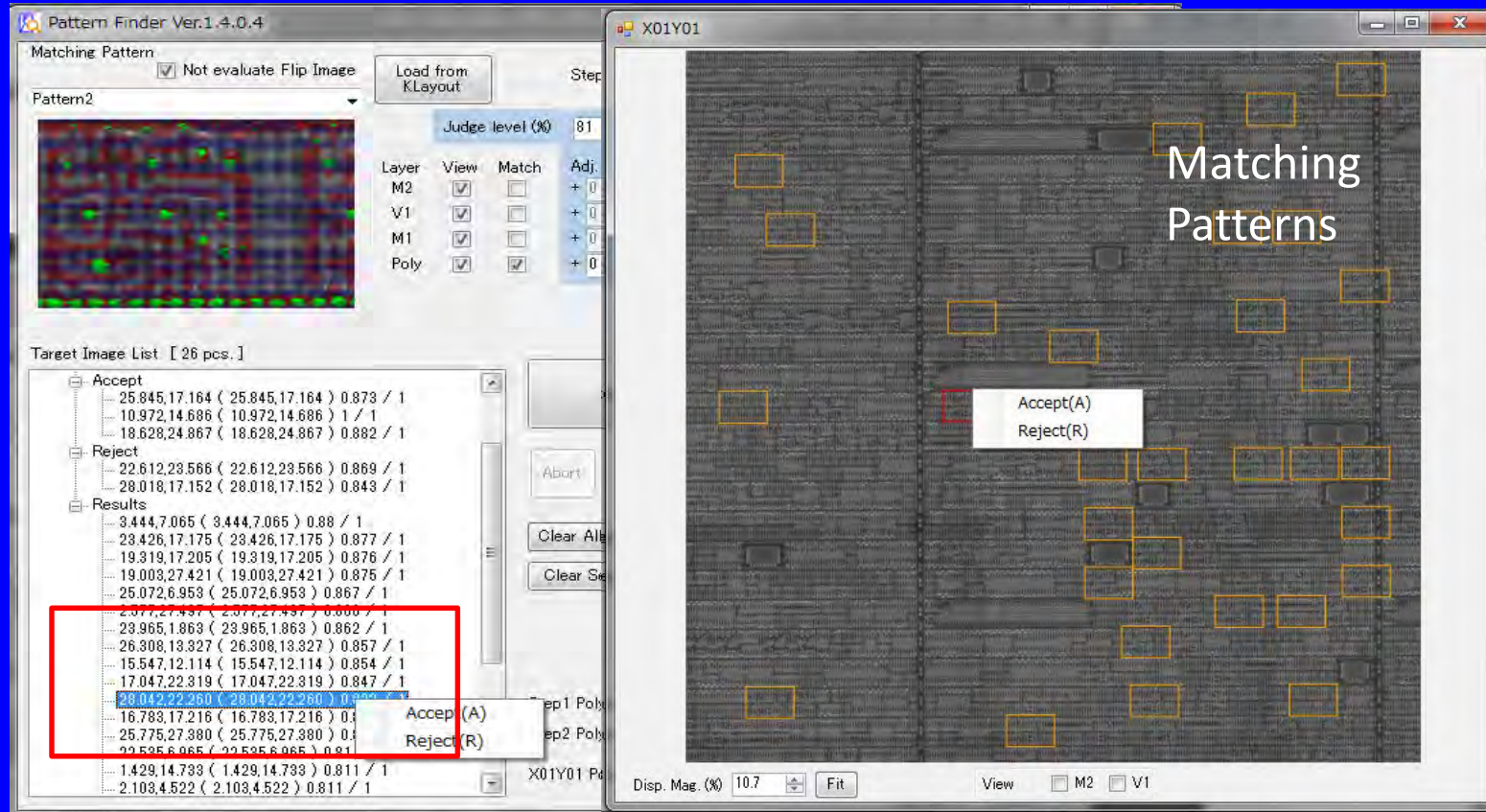
The screenshot shows the NetViewer software interface. On the left is a 3D PCB layout view of a circular board with various components. A yellow rectangular box highlights a specific component. On the right is a schematic diagram view showing electrical connections between components. A pink rectangular box highlights the same component in the schematic. A yellow arrow points from the highlighted component in the layout to the highlighted component in the schematic. A pink arrow points from the highlighted component in the schematic back to the highlighted component in the layout. In the center, there is a 'Layer List' panel with a list of layers (L0001 to L0008) and search options. At the bottom, there is a status bar showing coordinates and component ID: 51582, 104772 | U007.

# Pattern Matching Tool

Google search term: "youtube Ltec pattern matching"

<https://www.youtube.com/watch?v=Z2Vkgr3JWVw&list=PLe5EA9FhfOlwkxABwYRQ3jzPjKLhAO81P>

Target Pattern  
On SEM image  
or layout

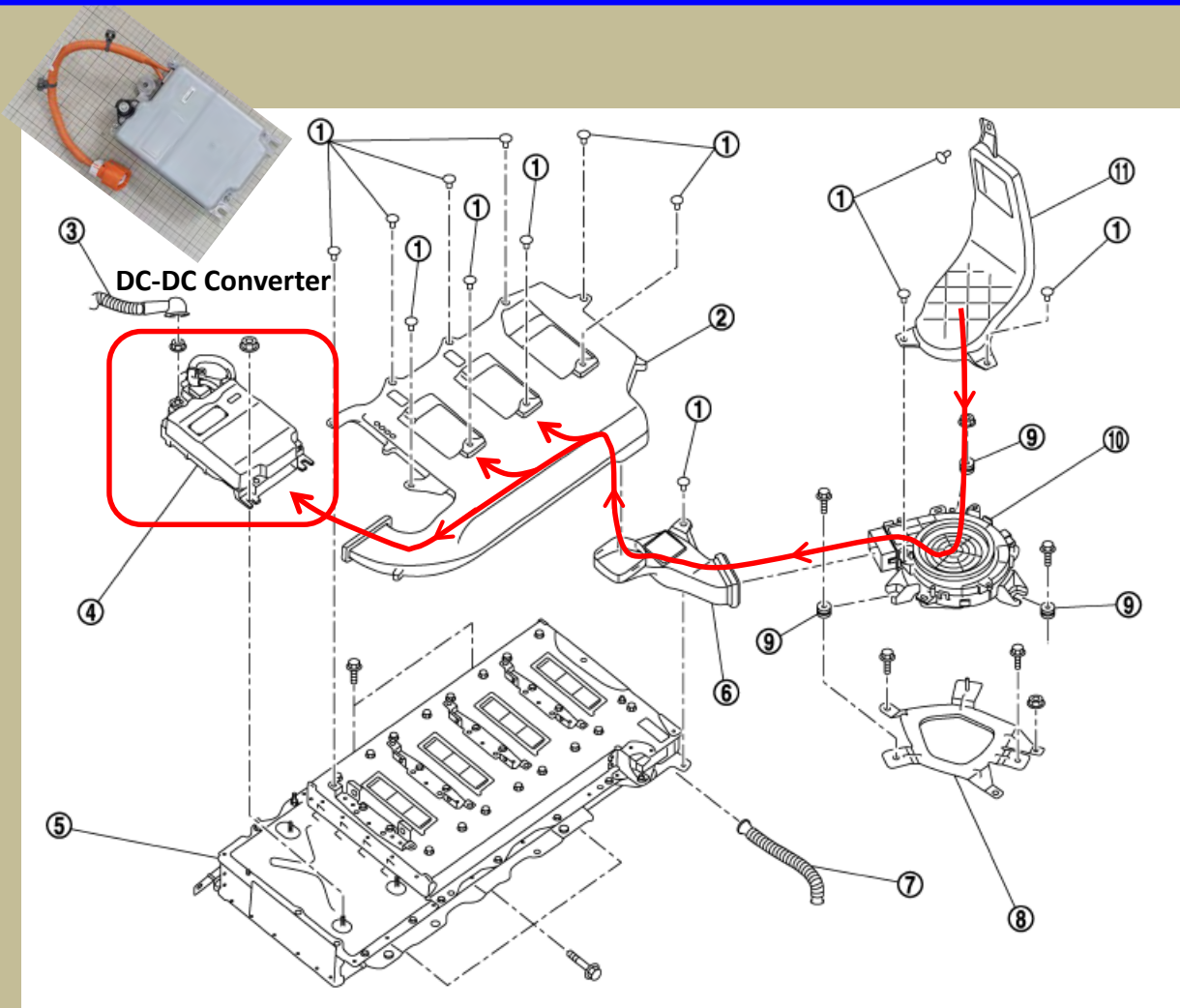


Potentially  
High \$ reward

*Helps identify infringing patterns*

# Modeling Mechanically and Electrically Integrated (Mechatronic) Systems (Example)

# Example: System-level Analysis



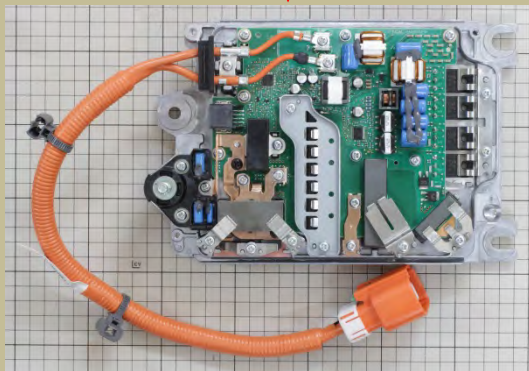
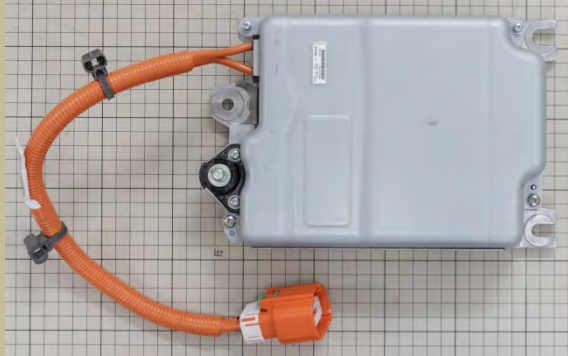
Air cooling system. The airflow is distributed to the DC-DC converter by the fan ⑩ through duct ②

2	Air duct1
4	DC/DC Converter supplies the 12V battery
5	Lithium-ion battery
6	Air duct 2
8	Battery cooling fan bracket
10	Battery cooling blower fan
11	Air duct 3

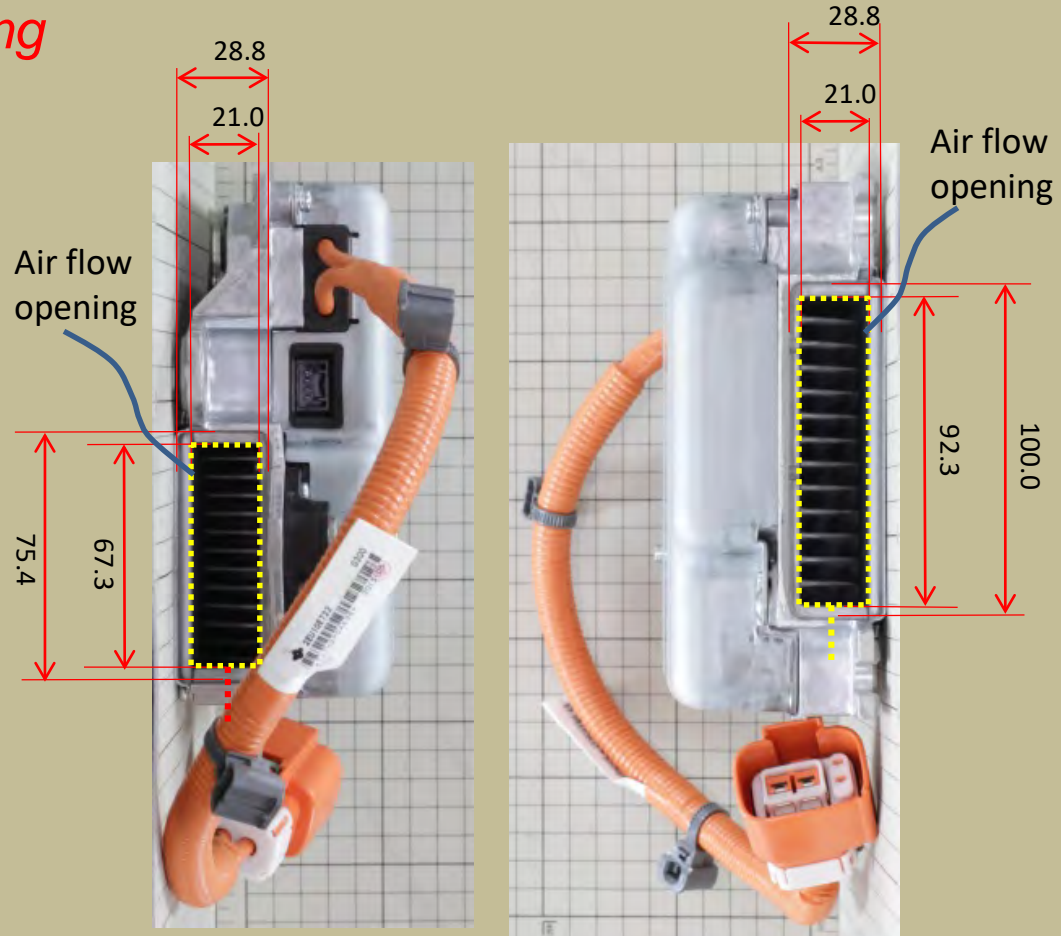
*Useful for  
electronic  
subsystem  
designers!*

# Why "Outsourced"? Example: "Mechatronics"

*We perform both RE and modeling*



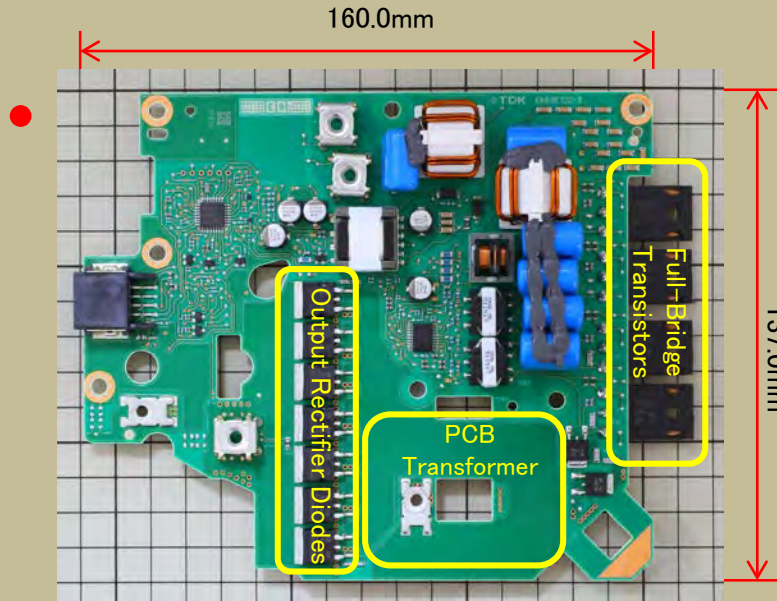
Images of the  
12V DC-DC converter



Air flow openings

*Objective: precise thermal modeling of the heatsink-device/component Interface*

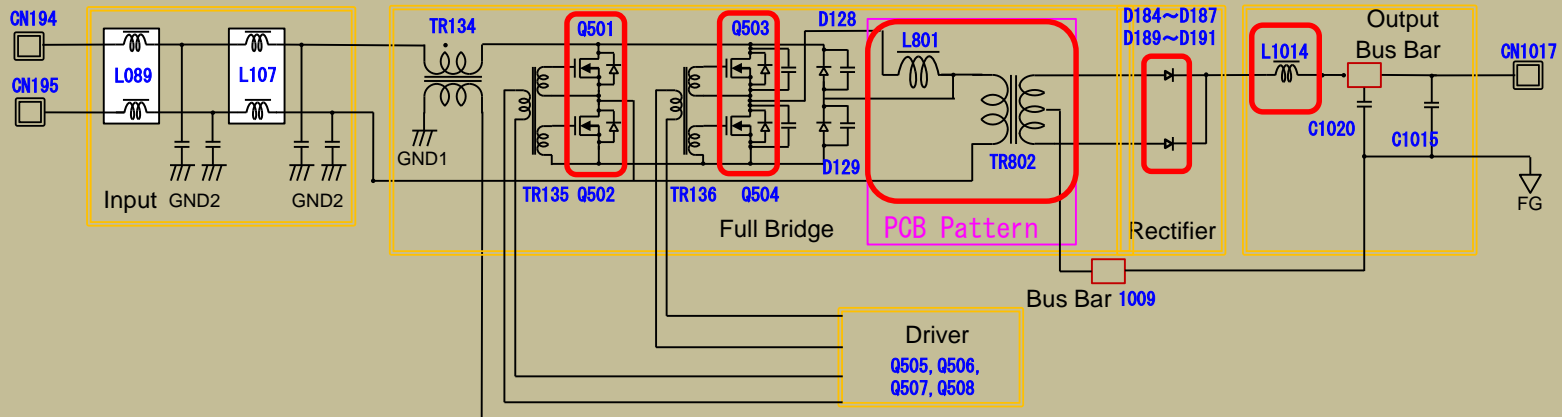
# Why "Outsourced"? Example: Mechatronics



Top View

DC-DC converter:  
PCB (after transformer removal)

*De-construction and preparation for modeling in the actual design environment*

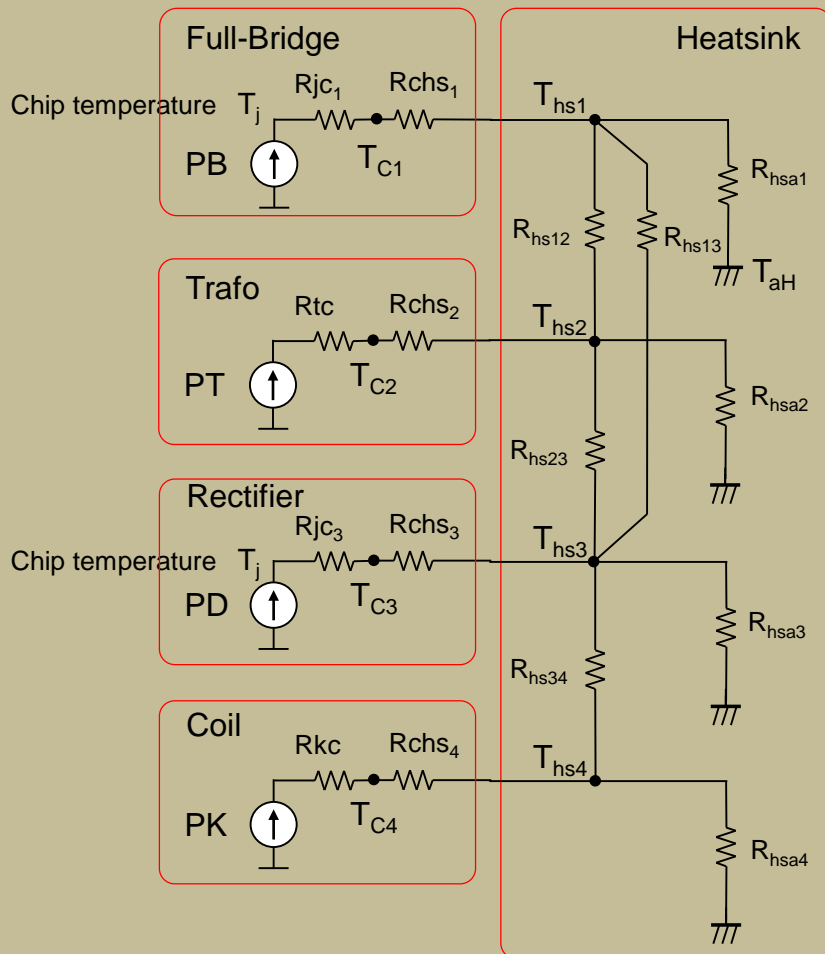


DC-DC converter circuit and its main heat sources.



# Model Development

## DC-DC Converter Thermal Network



Temperatures			
T <sub>j1</sub>	FB Transistors T <sub>j</sub>	100.6	°C
T <sub>j3</sub>	Rectifier Diodes T <sub>j</sub>	132.8	°C
T <sub>t</sub>	Transformer Temperature	90.6	°C
T <sub>k</sub>	Coil Temperature	111.6	°C
Ths1	FB Transistor-Heat sink interface	86.6	°C
Ths2	Transformer-Heat sink interface	84.6	°C
Ths3	Rectifier Diode-Heat sink interface	82.4	°C
Ths4	Coil Heat sink Interface	81.6	°C
TAVG	Heat sink Interface Average Temp	83.8	°C
R <sub>th, hs</sub>	Heat sink AVG thermal Resistance	0.48	°C/W
TaH	Ambient (Heatsink Fin surface) temperature	50	°C
PB	Full-Bridge power loss (k=4)	28	W
PD	Rectifier Diode dissipation	24	W
PT	Transformer power loss	12	W
PK	Output Coil power loss	6	W

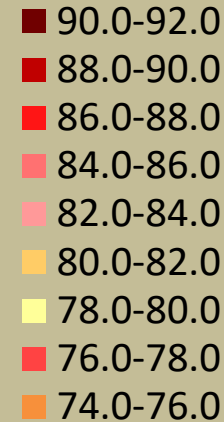
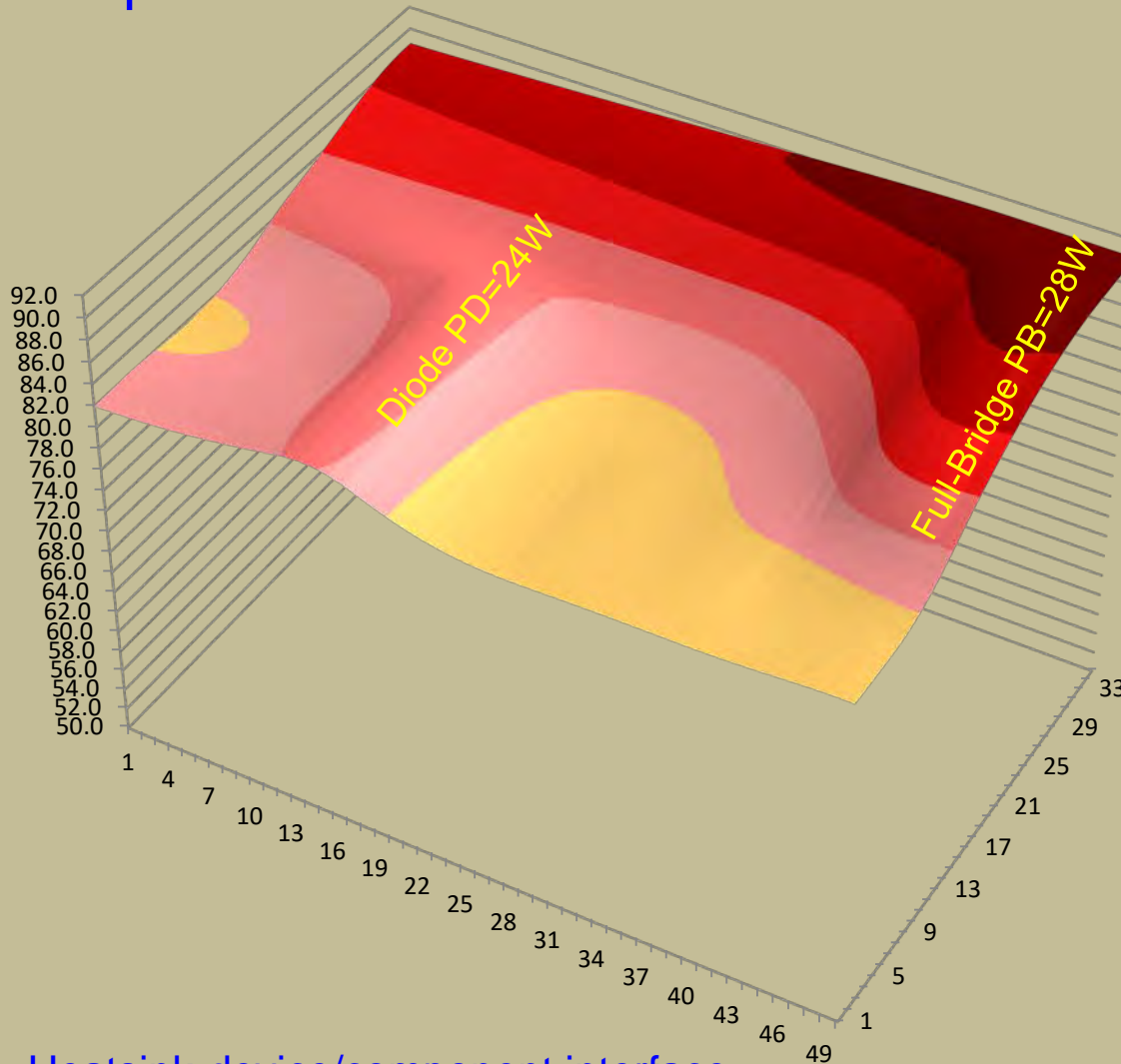
Estimated device/components' temperatures

Note the high T<sub>j</sub> value of the rectifier diodes

Network representation for the DC-DC converter.

# Why "Outsourced"? Example: Mechatronics

## Temperature Distribution Heatsink-device/component Interface



Heatsink-device/component interface

# Summary

- ❑ Deep RE is a complex labor-intensive process
- ❑ A highly competitive market, the emergence of high-temp. electronics, mechanical-electrical integration, new materials and methods, create the demand for Collaborative Outsourced Reverse Engineering (CORE)
- ❑ CORE
  - ❑ provides up-to-date competitive intelligence
  - ❑ provides direction to product development teams
  - ❑ enhances product positioning
  - ❑ effectively reduces the time to market
  - ❑ mitigates risks

# Summary (2)

- ❑ Collaborative Outsourced Reverse Engineering (CORE)
  - ❑ Provides expertise in performing deep analysis
  - ❑ Provides a broad horizon of visibility of the competitive landscape
  - ❑ Has proprietary tool set and unique know-how to enhance productivity
  - ❑ Facilitates close, dynamic, interactive, direct collaboration with product development teams

# Questions?



# More Questions?

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# Thank you!