

LTEC Corporation *Your most experienced partner in IP protection*

Microsemi APT80SM120B 1200V SiC MOSFET ANALYSIS REPORT

New

Release

November 2017. LTEC Corporation released a detailed structure and process analysis report of this 1200V silicon carbide MOSFET of Microsemi. This devise is the 1st 1200V product from



Package



SiC die

Device features

- Max. operating voltage: 1200V, rated DC Drain current ID=80A at Tj=25°C
- ON-resistance, RON x A= 1,076m Ω x mm²
- Double metal layer at Source PADs and Gate PADs is used in order to maximize the package density

The report has two individually purchasable sections: an 73-page Structure Analysis, and a 23-page Process Analysis section. The Structure Analysis section reveals the physical construction of the device, including EDX materials analysis, and many other fine details. The Process Analysis section includes manufacturing process flow, the estimated number of photomasking steps, and the impurity concentration of the epitaxial layer.

Structure analysis report:	\$4,000
Process analysis report:	\$4,000

Note: The listed report price may not be accurate as it decreases over time. Please contact us for current report pricing : **info@ltecusa.com**

17G-0019-1



LTEC Corporation US Representative Office No.203 2880 Zanker Road San Jose, CA 95034

Phone: (408) 432-7247 www.ltecusa.com Contact: info@ltecusa.com

Table of Contents Structure Analysis Report

	-
Device summary	
Table 1, Executive Summary	3
Analysis results	4
Table 2. Package structure overview	5
Table 3. Device structure: SiC MOSFET	6
Table 4. Device structure: Layer materials and thicknesses	7
Package overview	
X-ray	8
SIC MOSFT	
SiC MOSFET Analysis	10
Plain view (Optical Microscope)	11
Plain view, Scanning Electron Microscope (SEM)	21
Cross-sectional structure analysis (SEM)	29
Package structure analysis	
Detail structure	39
EDX material analysis	51

17G-0019-1

Page



Table of Contents Process Analysis Report

	Page
Analysis summary	3
Die	4
Die edge	5
Device structure SiC MOS FET	7
Transistor schematic diagram	
SiC MOSFET cell	
Plain view	8
(a) Die schematic diagram	
(b) Layout pattern schematic diagram	
SiC MOS FET front-end wafer process flow (estimated)	16
SiC JFET process sequence cross-sectional view	17
Relationship between device structure and electrical characteristic	20
Appendix	23
Relevant references	

Relevant patents

17G-0019-1

