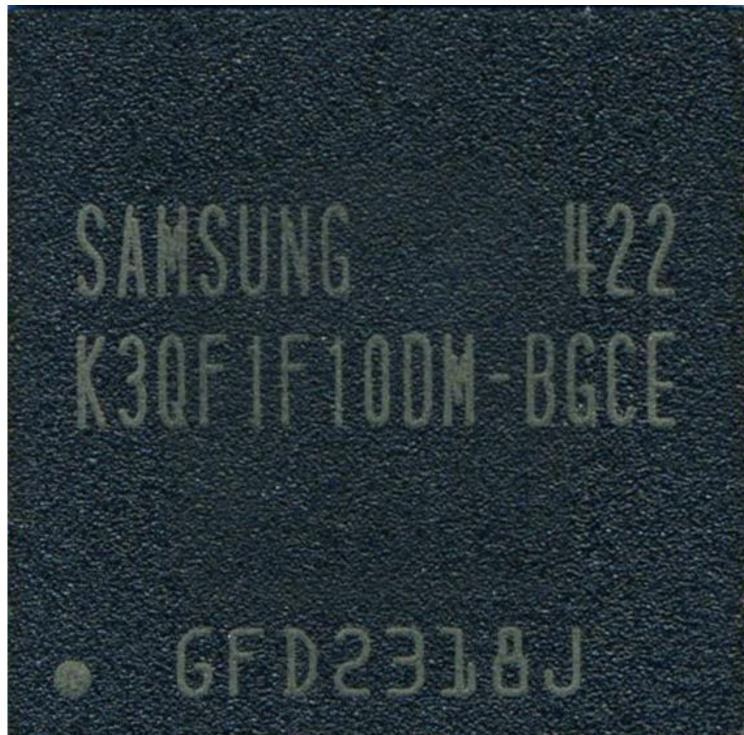
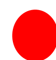
Semiconductor detail analysis sample report

LTEC Corporation

ITEM	ATOM Z3480	LPDDR3***
Manufacturer	Intel	SAMSUNG
Device Type	Processor for smartphone	DRAM
Package Marking	iⓂ© 12 Q415B475 SR1WS e1	SAMSUNG 422 K3QF1F10DM-BGCE GFD23L8J
Package Type	796-BGA	216-BGA
Die Marking	TNG ⒸⓂ intel 2012	-----
Clock speed	2.133 GHz	
Die Size	12mm x 12mm = 144mm2	-----
Die Thickness(μm)	212	77
Process	22nm 1 mtalgate – 9 Metal + 1 LI Tri-Gate CMOS High-k MTG, M1-M8 Cu dual damascene, M0(LI) wangsten	-----
Application	Smartphone	-----
Fab	Intel Fab Hillsboro / Chandler / Qiryat Gat	-----

Package size : 12mm×12mm=144mm^2



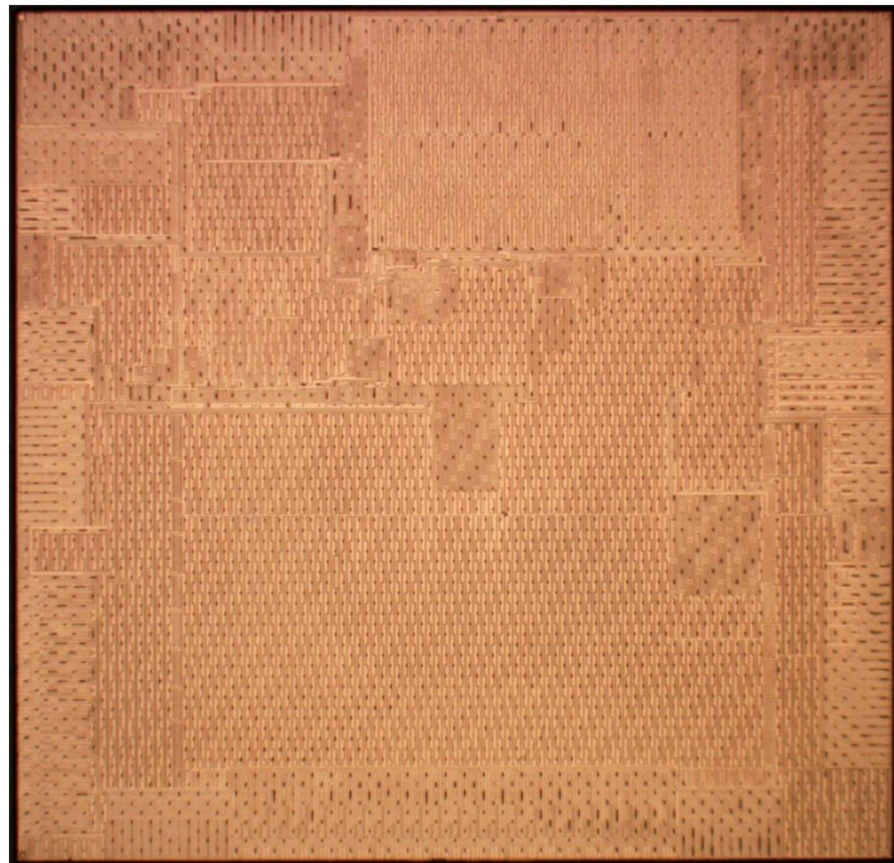


Package Top-View

Package size : 12mm × 12mm=144mm^2

Package Top-View 1mm

Die size : 9.00mm × 8.73mm=78.57mm^2



Die Top-View （Top metal layer) 1mm

Intel® Atom™ Processor Z3480

・Die Marking

Intel® Atom™ Processor Z3480

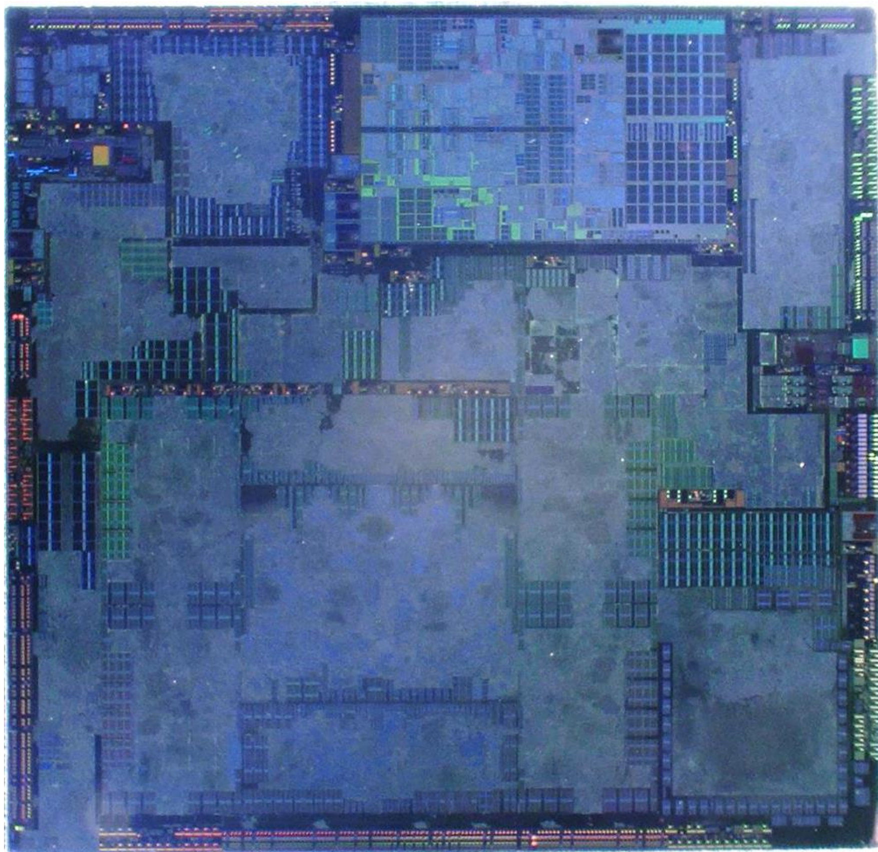
Rotation 90°

10μm

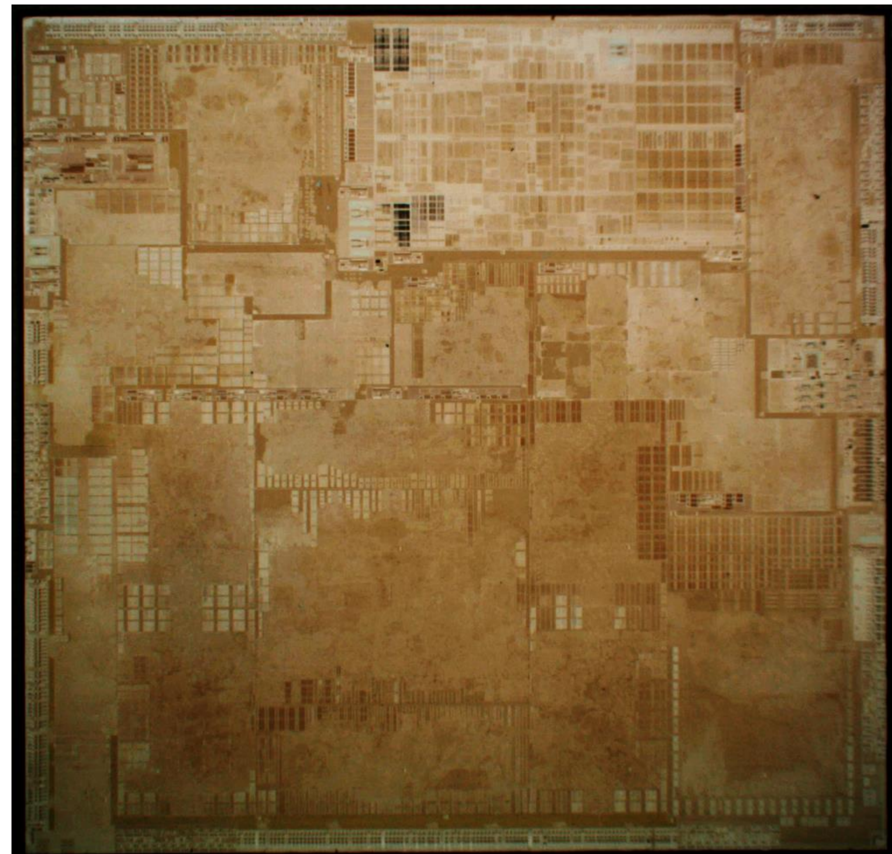
Die Markings (M8 layer)

Die Top-View (M8 layer)

1mm



Die Top-View （M0/Metal gate layer)



Die Top-View （Diffusion layer)

5-1-6. M1-M8 interconnect

- It is estimated that M1 to M6 inter layers are used a ultra low-k (ULK) carbon-doped oxide (CDO).
- Also, it is estimated that M7 and M8 inter layers are used a low-k CDO.
- Air-gap technology was not used. (IBM use air-gap technology in 22nm-node)
  It is estimated that Intel will use air-gap technology in 14nm-node.

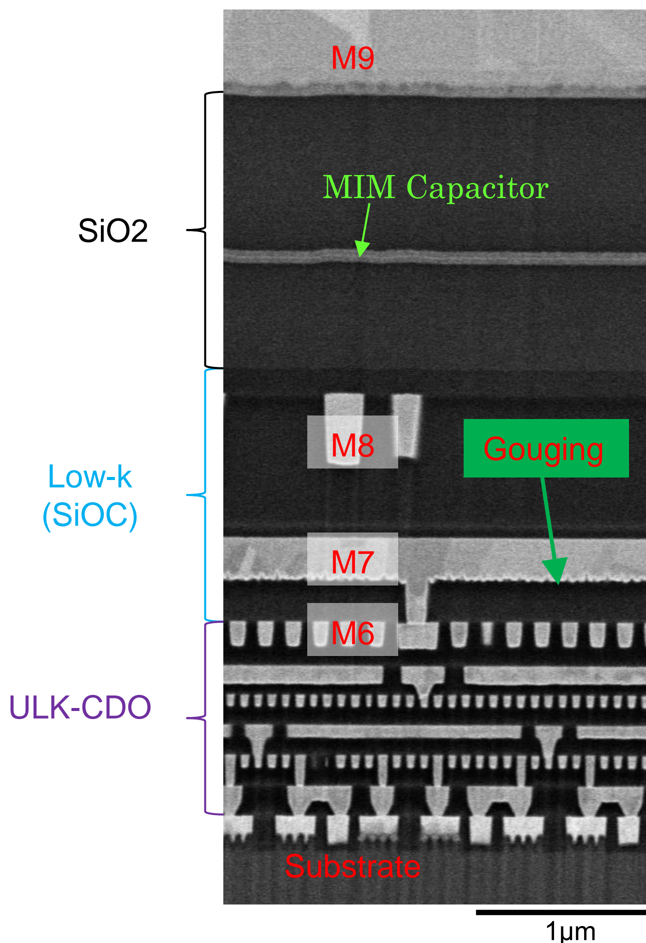


Fig 5-1-6-1 SEM cross section

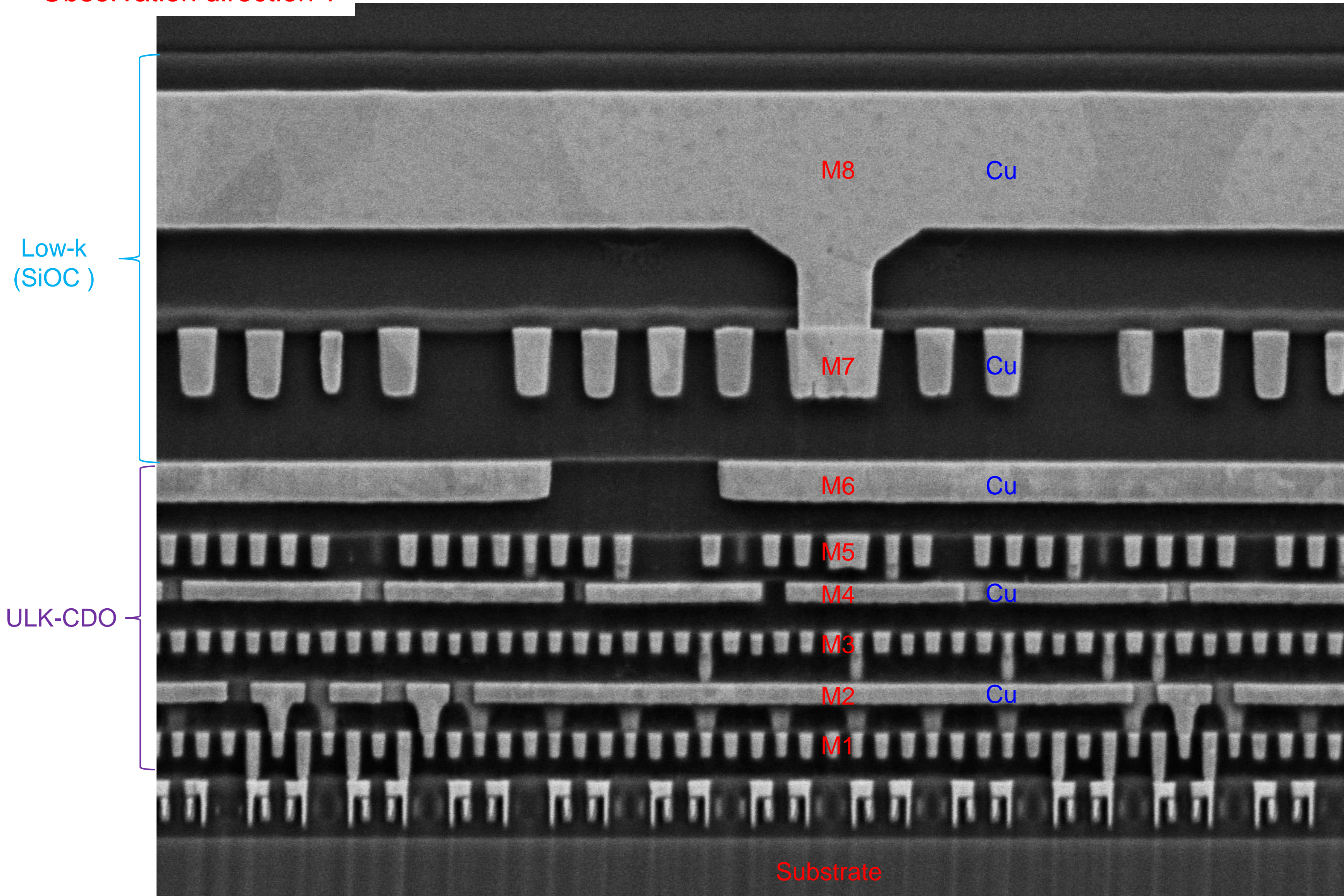
Table5-1-6-1 Measurement results summary

Measuring point	Thickness (nm)	W/S (nm) ※	Pitch (nm)
M9~MIM~M8 inter layer	1653	—	—
M8 layer	383	230／130	360
M8~M7 inter layer	383	—	—
M7 layer	230	140／100	240
M7~M6 inter layer	210	—	—
M6 layer	135	100／60	160
M6~M5 inter layer	110	—	—
M5 layer	103	66／46	112
M5~M4 inter layer	64	—	—
M4 layer	64	45／35	80
M4~M3 inter layer	112	—	—
M3 layer	76	45／35	80
M3~M2 inter layer	94	—	—
M2 layer	70	45／35	80
M2~M1 inter layer	102	—	—
M1 layer	85	55／35	90
M1~M0 inter layer	74	—	—
M0 layer	66	—	—

ULK-CDO enable interconnections to be narrower.

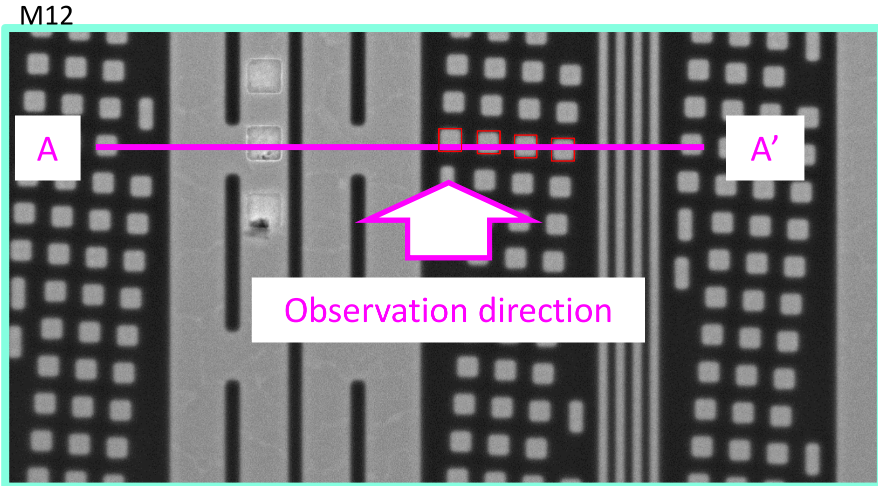
※W/S : (Minimum) Width / (Minimum) Spacing

Observation direction 1



* All device materials were estimated.

Fig. 5-11-5 SEM cross section (logic area, Observation direction 1)



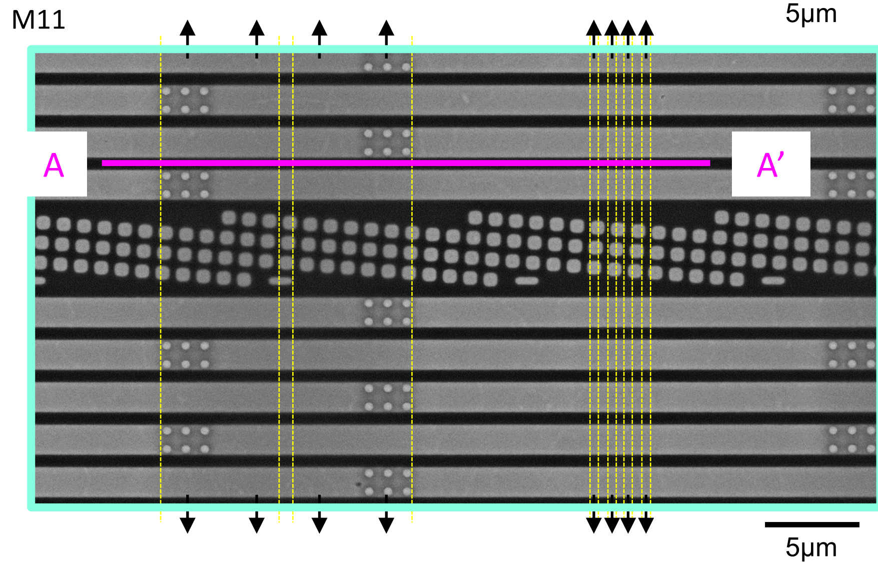


Fig.7.3. Cross-section observation point (Area#A-1)

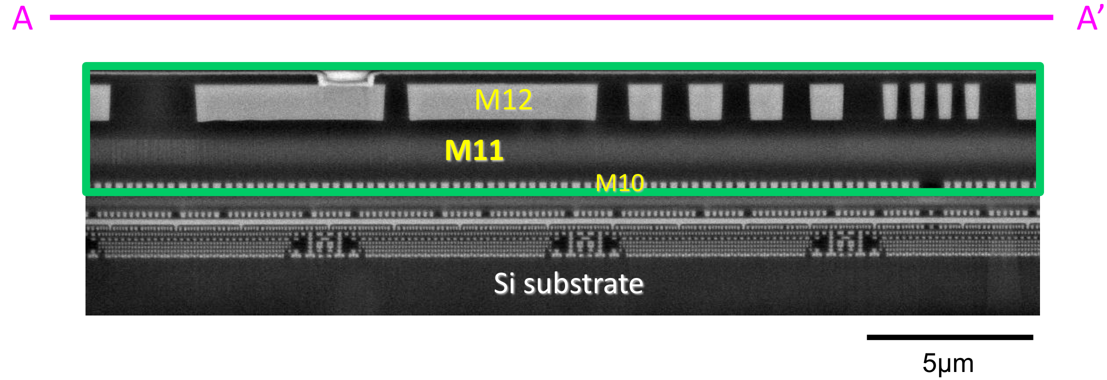


Fig.7.4 SEM, Cross-section (Area#A-1, A-A')

8. EDX scan for the cross-section

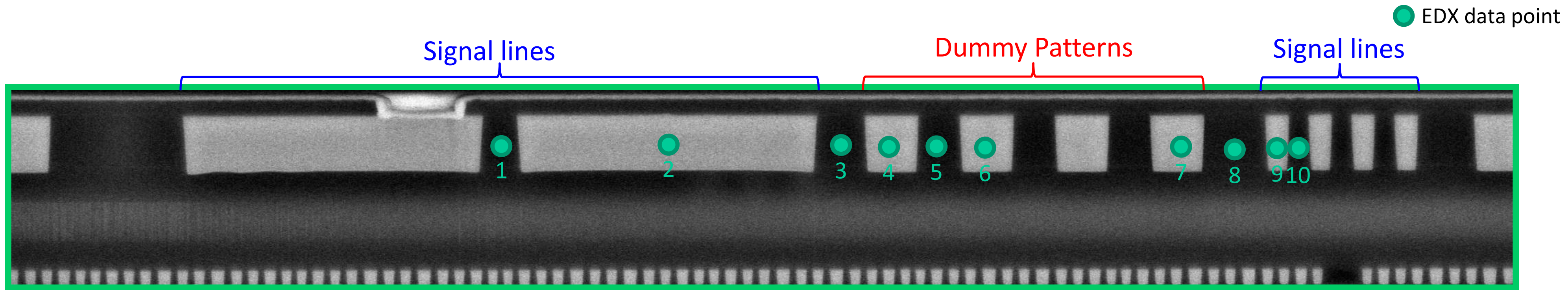
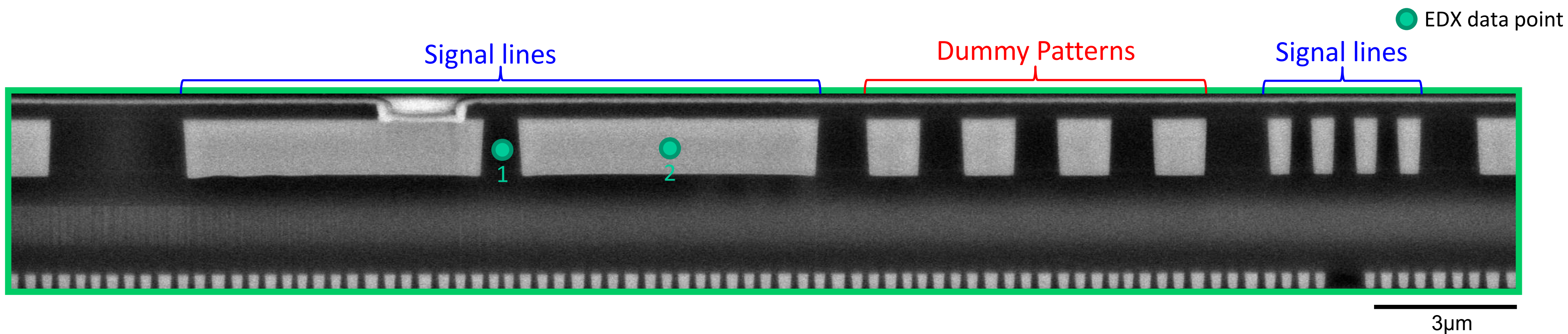


Fig.8.1 EDX data points

P9

Table 8.1 EDX scan results

EDX data No.	EDX result
1	Silicon oxide
2	Cu
3	Silicon oxide
4	Cu
5	Silicon oxide
6	Cu
7	Cu
8	Silicon oxide
9	Cu
10	Silicon oxide



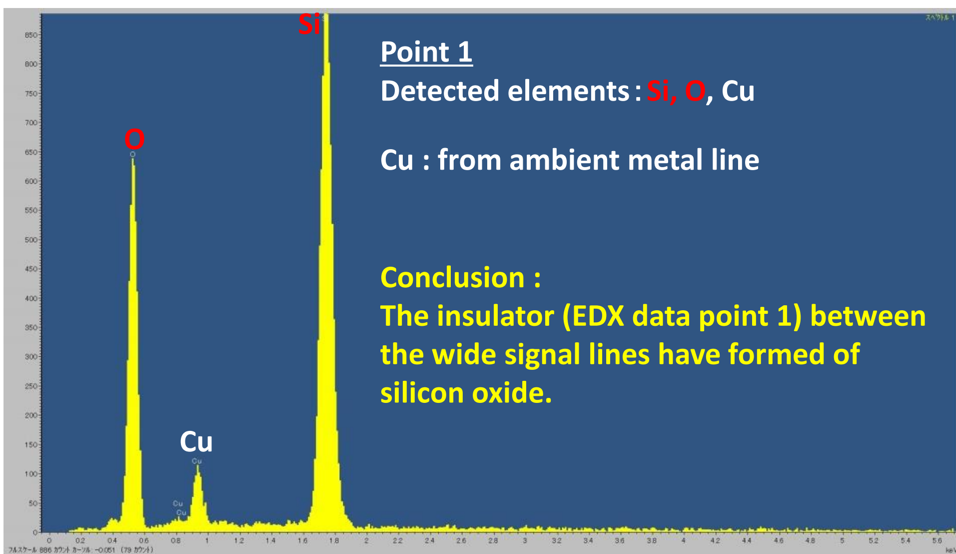


Fig.8.2 EDX spectrum (EDX data point 1)

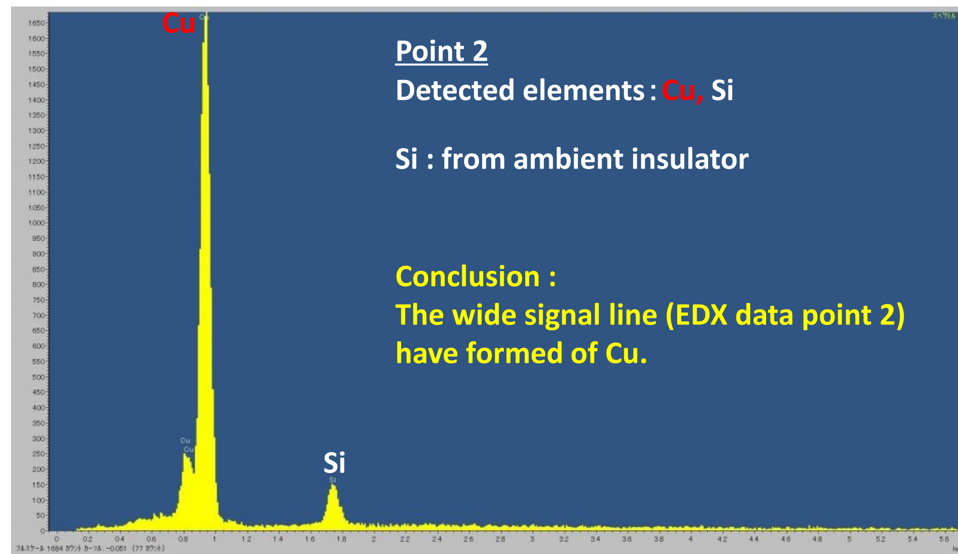


Fig.8.3 EDX spectrum (EDX data point 2)

5-1-1. Fin FET (1/2)

- Intel's 22nm bulk fin FET (Tri-gate) technology was used.
- Fin was formed of Si. (Si-Ge fin may be found in future generation)
- It is estimated that Si-fin is grown epitaxially.
  - Crystal Mismatch of epi - Si substrate interface was not found. It is estimated that epitaxial growth is perfect at the epi - substrate interface.

P12

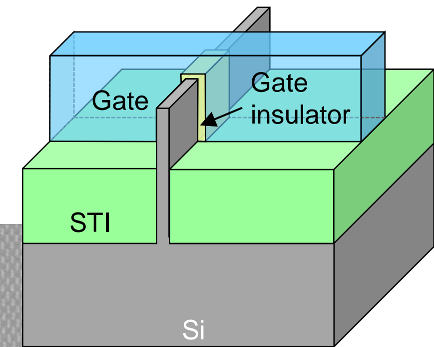


Fig. 5-1-1-1
Perspective view of fin FET

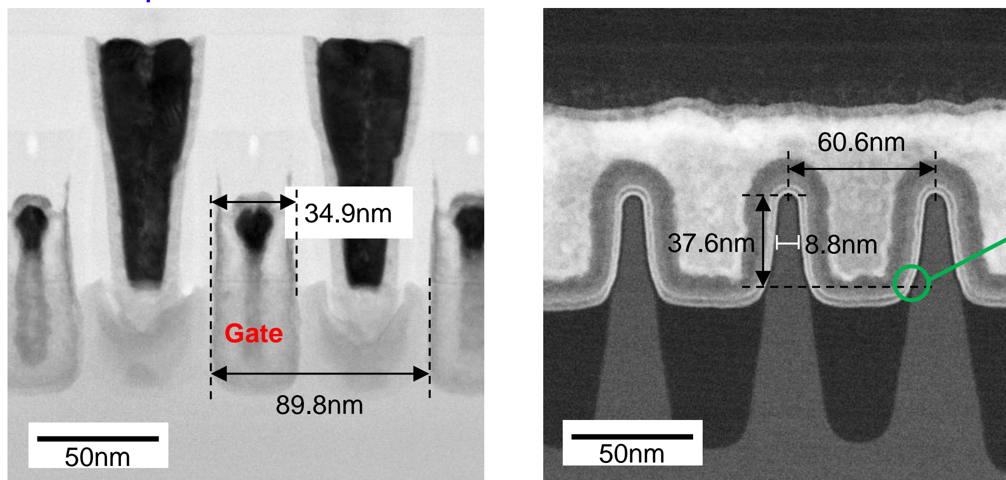


Fig. 5-1-1-2 STEM cross section (GPU Logic PMOS)

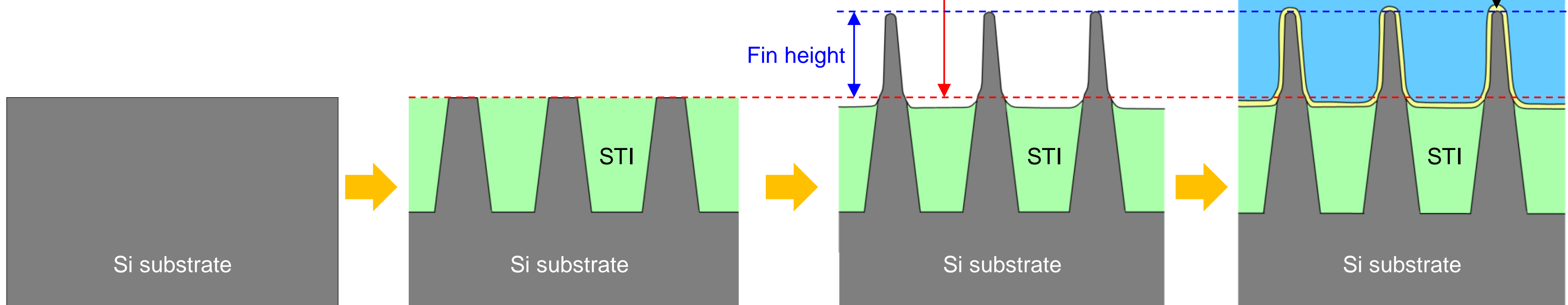


Fig. 5-1-1-3 Fin FET process flow (estimation)

5-1-1. Fin FET (2/2)

- Lgate of HV MOS and I/O Logic were longer than other transistors.
- SiOx of HV MOS and I/O Logic were longer than other transistors.
- It is estimated that SiOx of HV MOS and I/O Logic are thicker to get high breakdown voltage.

Table5-1-1-1 Measurement results summary (PMOS)

Transistor type	Lgate (nm)	Gate pitch (nm)	Fin Height (nm)	Fin Width (nm)	SiOx gate insulator (nm)	HfOx gate insulator (nm)
GPU Logic	34.9	89.8	37.6	8.8	1.1	1.1
High Voltage	155.6	270.7	35.0	9.4	4.9	1.9
Power switch	32.3	90.4	36.4	9.2	0.9	1.3
Decoupling capacitor	—	—	—	—	—	—
IO Logic	155.1	277.6	34.2	8.4	5.1	1.6

Table5-1-1-2 Measurement results summary (NMOS)

Transistor type	Lgate (nm)	Gate pitch (nm)	Fin Height (nm)	Fin Width (nm)	SiOx gate insulator (nm)	HfOx gate insulator (nm)
GPU Logic	26.7	90.8	36.7	8.8	1.3	1.2
High voltage	153.2	273.8	34.7	9.2	4.4	2.0
Power switch	—	—	—	—	—	—
Decoupling capacitor	29.5	90.8	35.0	9.2	1.5	2.1
IO Logic	156.7	268.7	34.4	7.7	4.9	1.6

5-1-2. High-k/metal gate for LP/ULP transistor (2/2)

- TiN / TaN (or TaOx) / TiN / TiAlON(C) / TiN stack modulates work function in POMS.
- TiN / TaN (or TaOx) / TiAlON / TiAlO(C) / TiN stack modulates work function in NOMS.
- High-k dielectric material was HfOx. (It is not other High-k material like HfSiOx and La2O3.)
- SiOx gate insulator was intercalated to control boundary with Si.

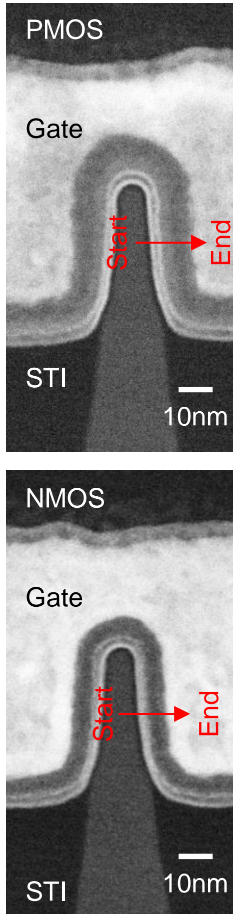


Fig. 5-1-2-3 EELS analysis line

EELS analysis line
Start
End

【PMOS】

C N O Ti Al Hf Ta W Si

W
TiN:2.5nm
TiAlON(C):3.4nm
TiN:3.0nm
TaN (or TaOx) :1.5nm
HfOx:1.3nm
SiOx:0.8nm
Si
TiN:0.6 nm

distance (nm)
intensity (a.u)
5x10^6

【NMOS】

C N O Ti Al Hf Ta W Si

W
TiN:1.9 nm
TiAlO(C):3.2 nm
TiAlON:0.6 nm
TaN (or TaOx):0.8 nm
HfOx:1.5 nm
SiOx:0.8 nm
Si
TiN:0.4 nm

distance (nm)
intensity (a.u)
5x10^6

Fig. 5-1-2-4 Logic transistor EELS results, PMOS (left) and NMOS (right)

5-1-7. Inductor

- There were two identical spiral inductors on the die.
- Spiral inductors were formed by thick top metal (M9) layer.

Table5-1-7-1 Measurement results summary

Inductor-No.	Layer	T :Thickness (μm)	Turn number	W :Width of line (μm)	S :Spacing(μm)	l_x / l_y :Side length (μm)
1	M9/M8	—	4	7.71(Top)/ —	6.59(Top)/ —	125.75 / 144.00
2	M9/M8	6.70	4	7.71(Top)/8.18(Bottom)	6.59(Top)/6.12(Bottom)	125.75 / 144.00

M9:Main line, M8:Connection line

Minimum pitch 1.43μm (M9-layer)

Cross-section A-A'

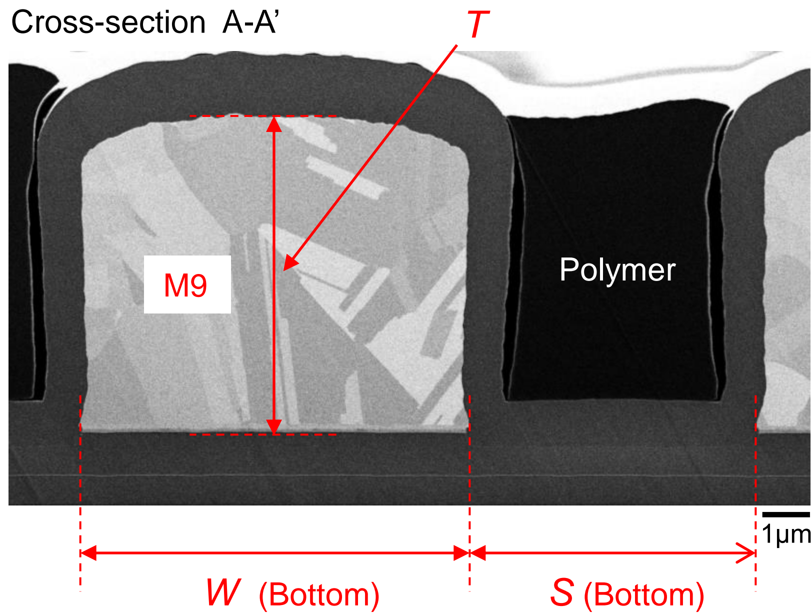


Fig. 5-1-7-1 SEM cross section (Inductor area)

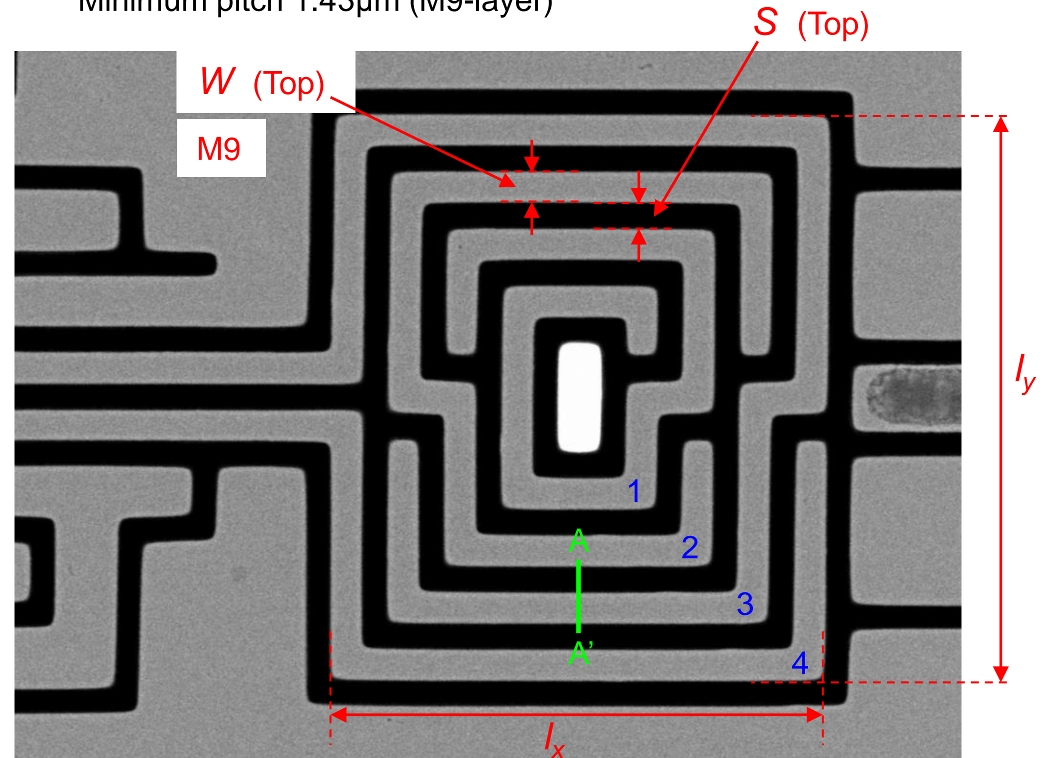


Fig. 5-1-7-2 SEM plan-view (M9)

5-1-8. High density MIM capacitor

- Thin MIM capacitors were formed between M8 and M9.
- MIM capacitors covered the entire die area.
- Upper and lower electrodes were about 10nm thinner than CORE i5-4430 Haswell (another Intel's 22nm product).

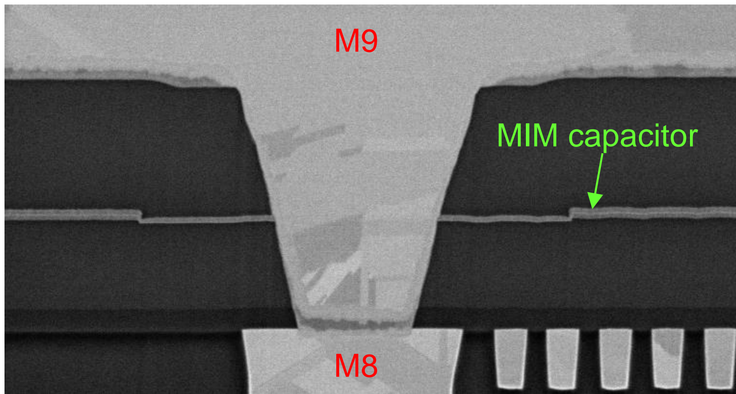


Fig. 5-1-8-1 SEM cross section

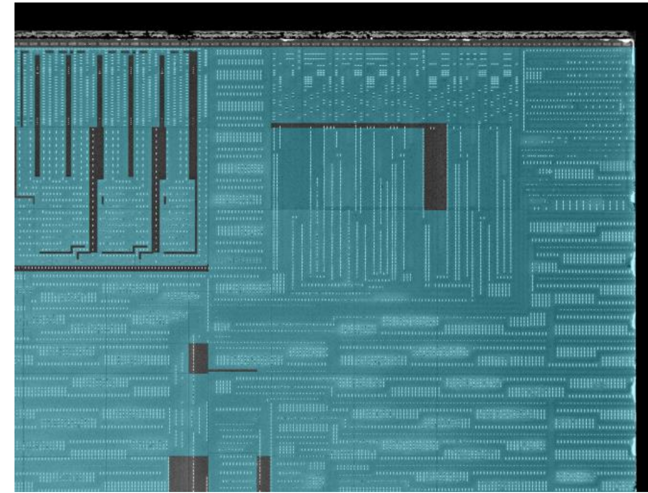


Fig. 5-1-8-2 SEM plan-view (MIM layer)

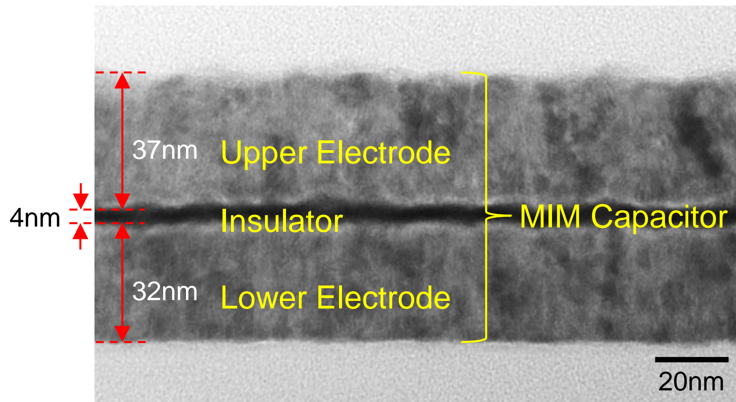


Fig. 5-1-8-3 TEM cross section (MIM, Z3480 Merrifield)

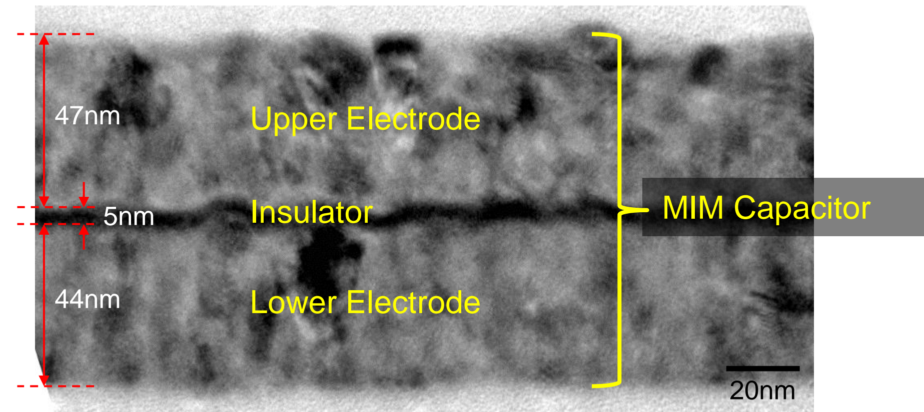
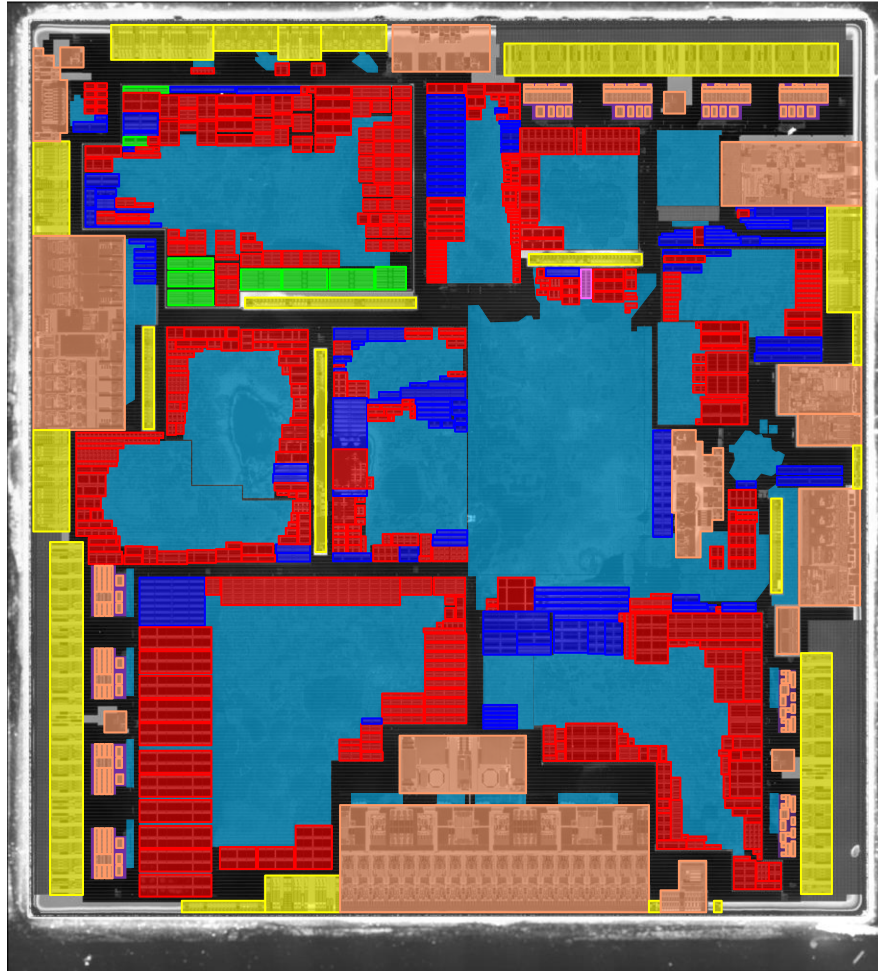


Fig. 5-1-8-4 TEM cross section (MIM, CORE i5-4430 Haswell)

Block area ratio calculation
(28nm processor)

● 1Pin



●

- 6Tr.SP-SRAM
- 8Tr.DP-SRAM
- 10Tr.DP-SRAM
- ROM
- Logic1
- Logic2
- Analog
- I/O

Table 6-4-1 Area ratio

Blocks	Total area [x10^{3}µm^2]	Area ratio [%]
Logic 1	17,250	29.94
Logic 2	530	0.92
6Tr.SP-SRAM	8,220	14.27
8Tr.DP-SRAM	2,580	4.48
10Tr.DP-SRAM	400	0.69
ROM	21	0.04
Analog	7,700	13.37
I/O	4,450	7.72
Scribe/Blanc	16,459	28.57
Total	57,610	100

5-1-9. SRAM

- Low voltage 6T-SRAM was selected * .
- Two types of 8T-SRAM having different 1bit cell size were found.

* Intel published three types of 6T-SRAM for 22nm-node at IEDM 2012.
  - High density / low leakage (HD) : 1bit cell size 0.092μm^2
  - Low voltage (LV) : 1bit cell size 0.108μm^2
  - High performance (HP) : 1bit cell size 0.130μm^2

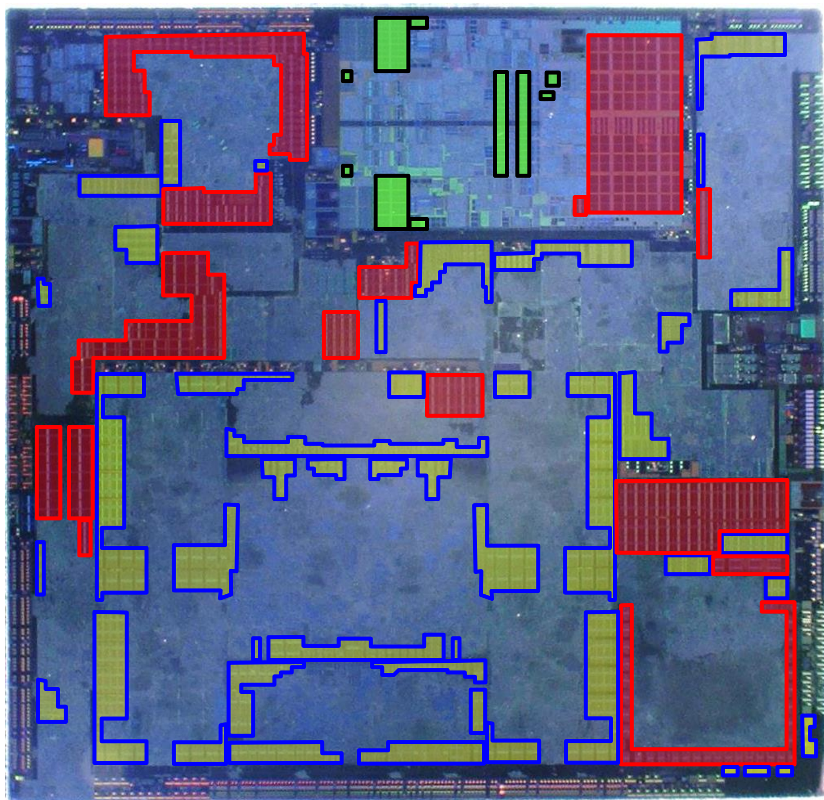


Fig. 5-1-9-1 Die Top-view (Memory IP)

6T-SRAM (LV) 1bit cell size : 0.60μm × 0.18μm = 0.108μm^2

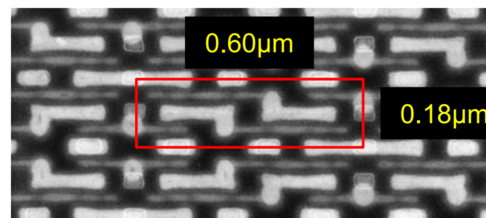


Fig. 5-1-9-2 LV 6T-SRAM

8T-SRAM (1) 1bit cell size : 1.53μm × 0.19μm = 0.290μm^2

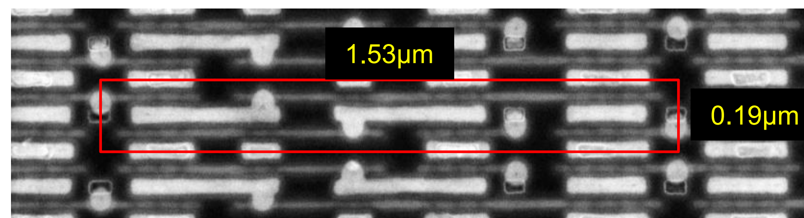


Fig. 5-1-9-3 8T-SRAM (1)

8T-SRAM (2) 1bit cell size : 1.60μm × 0.19μm = 0.304μm^2

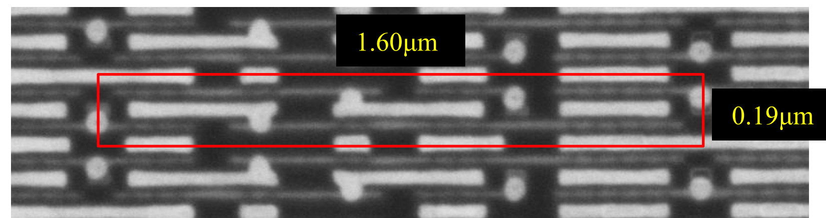
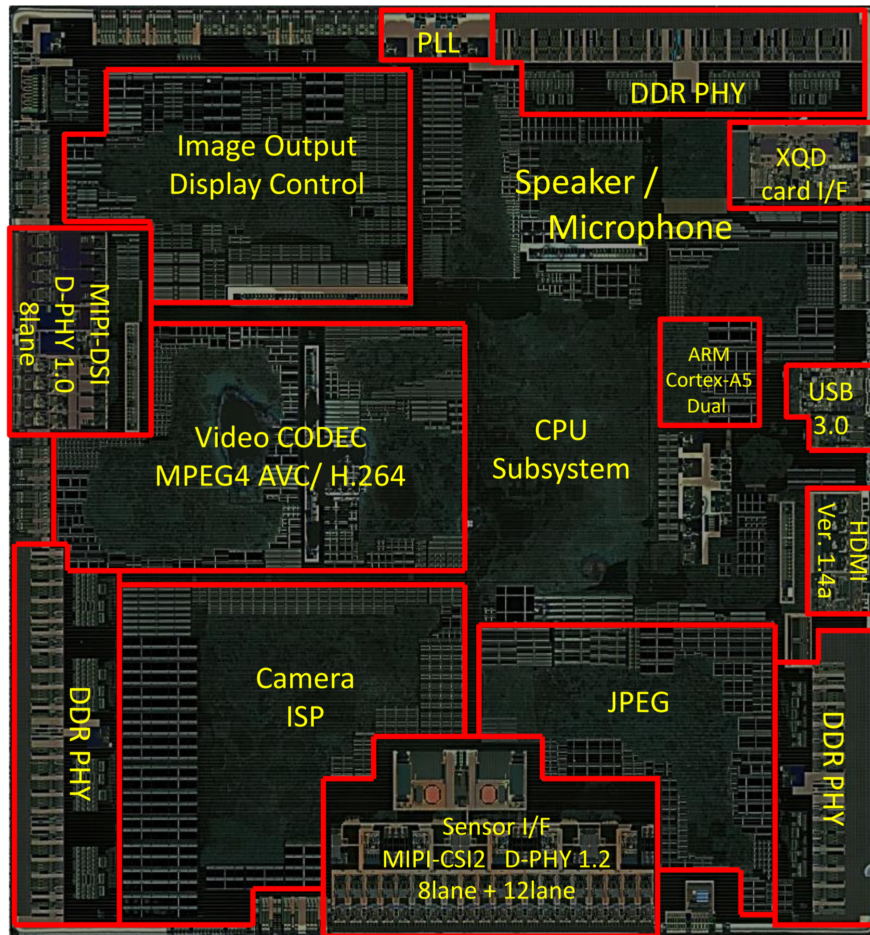


Fig. 5-1-9-4 8T-SRAM (2)

Function block identification
(28nm processor)

1Pin



Function block	Area [mm^2]
CPU(ARM Cortex-A5 Dual)	0.72
JPEG	3.81
ISP	6.18
Video CODEC	6.26
Image Output Control (Display)	5.00
DDR PHY	7.04
HDMI	0.57
USB 3.0	0.49
XQD card I/F	0.80
MIPI-CSI2	4.11
MIPI-DSI	2.57
PLL	0.38

5-1-10. Via

- Borderless via technology was used within M8 to M1.
- Overlap margin was minus in bottom of borderless via (via wider than metal line).
- It is estimated that borderless via contributes to shrink die size.

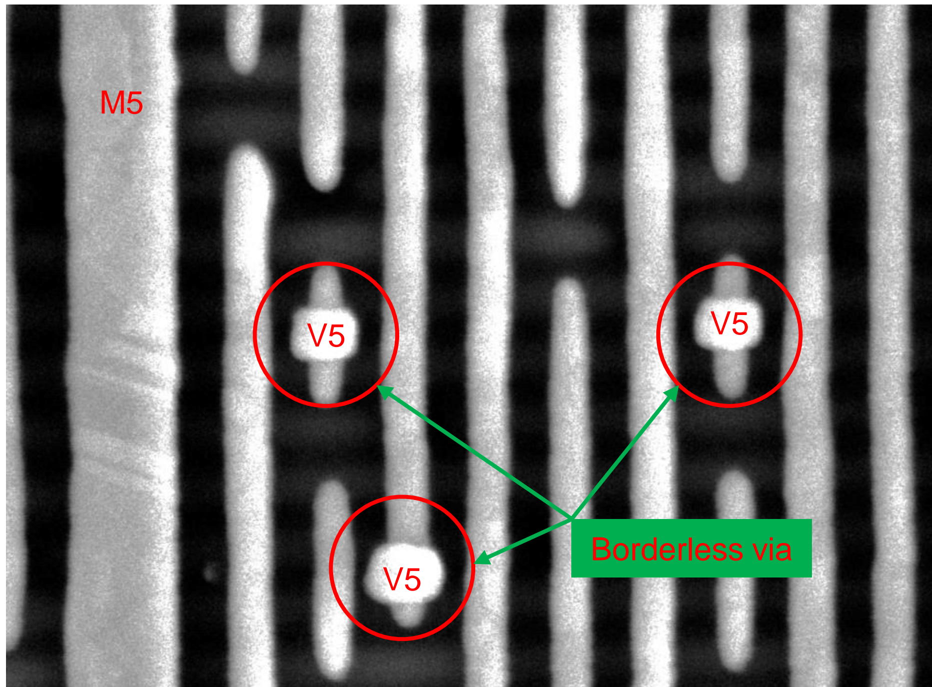


Fig. 5-1-10-1 SEM plan-view (M5)

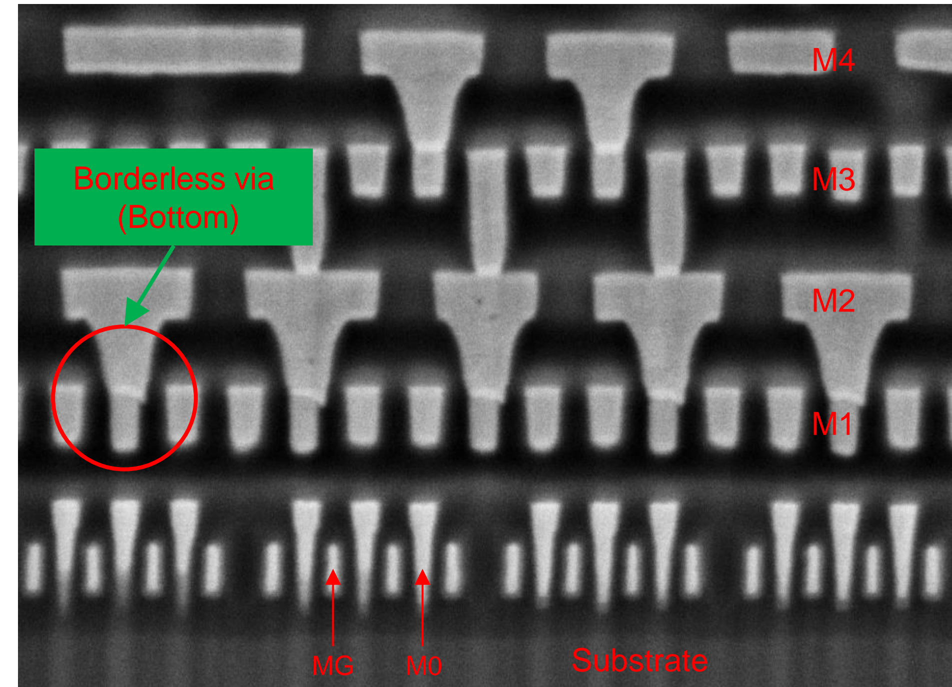


Fig. 5-1-10-2 SEM cross section (logic area)

MG; Metal gate

5-10. Diffusion profiles

- Channel stop implant region width was narrower than STI width.
- Power switch cell n-well and Logic n-well were equally doped.
- N-well didn't continue between power switch cell and logic area

Fig. 5-10-1 Die Top-View (Diffusion layer)

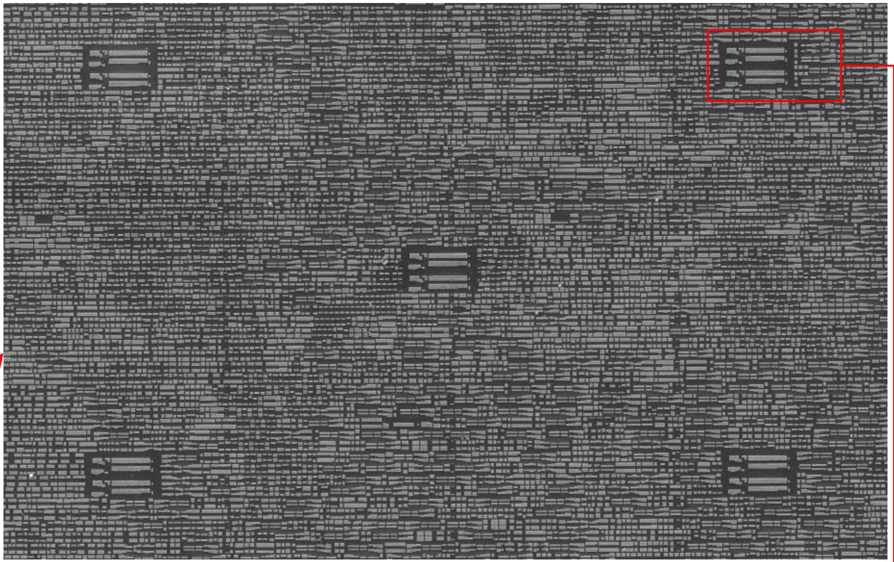


Fig. x-x-2 SEM Top-View (Diffusion layer)

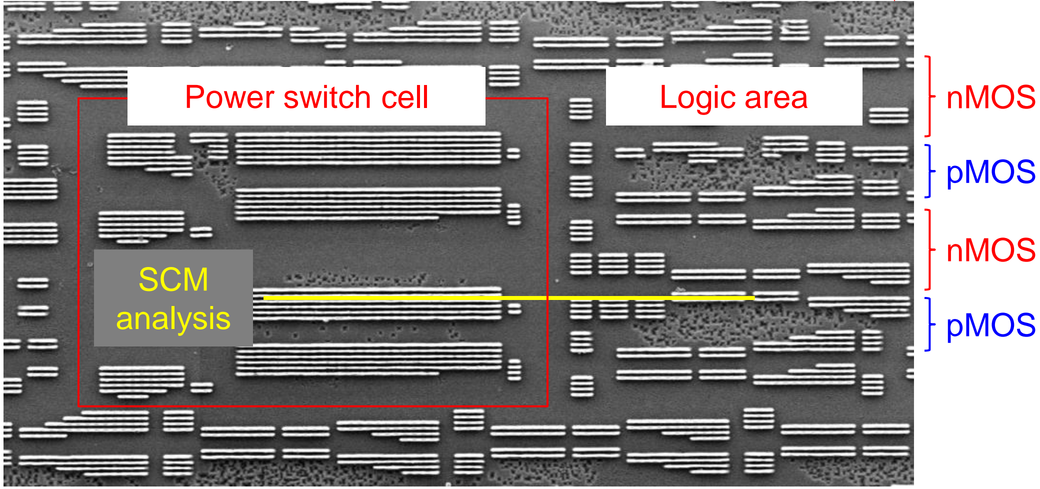


Fig. 5-10-2 SCM analysis Point

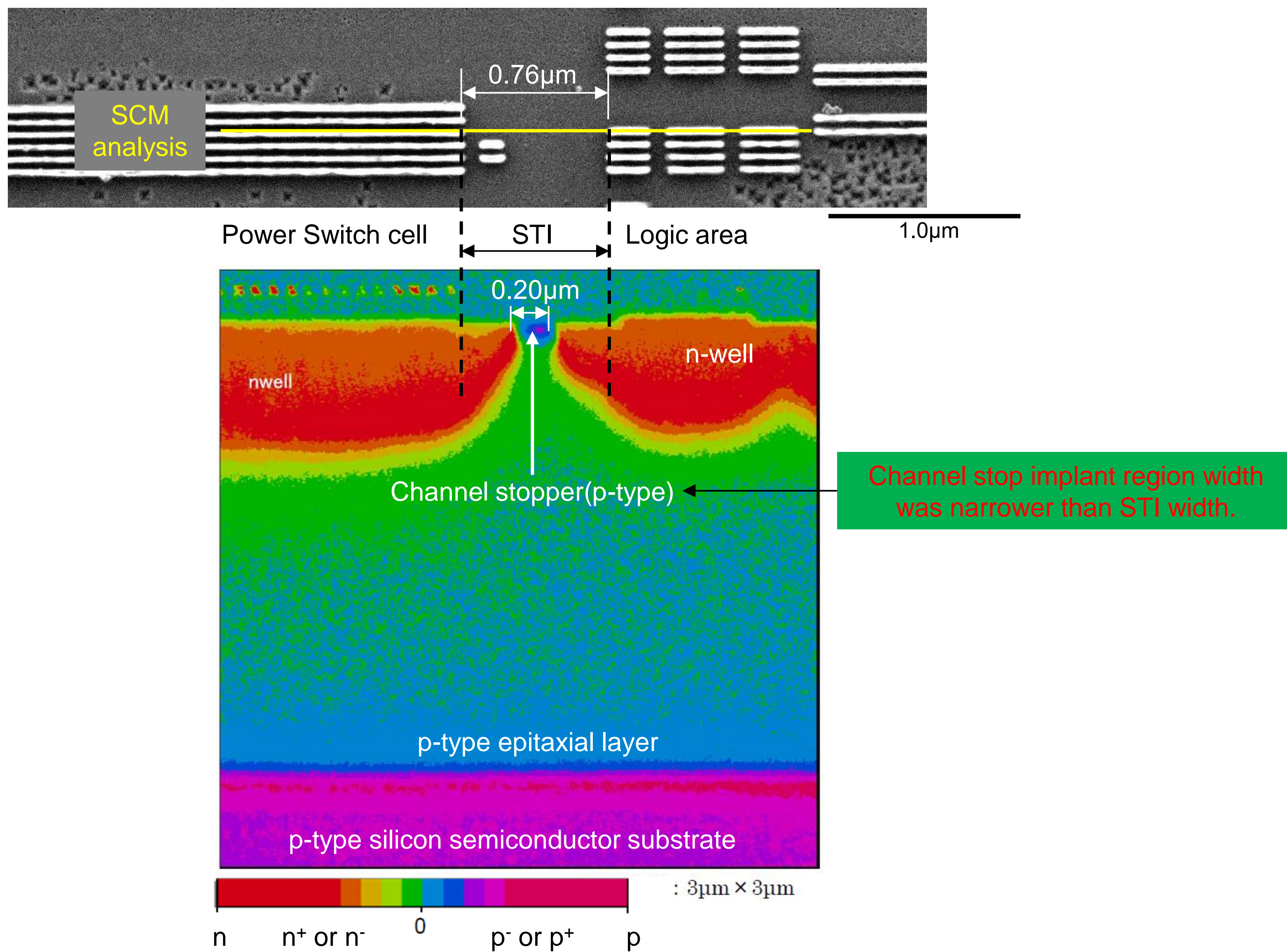


Fig. 5-10-3 SCM dC/dV image

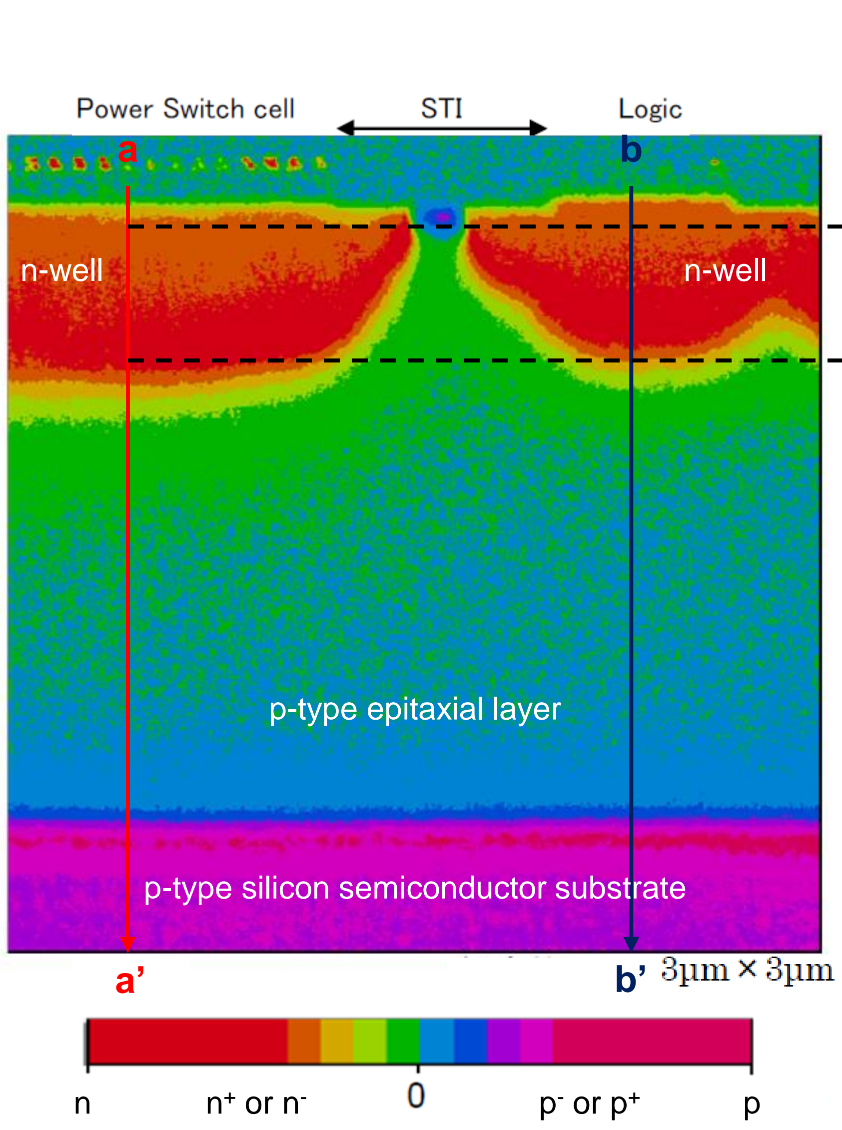


Fig. 5-10-4 SCM dC/dV image

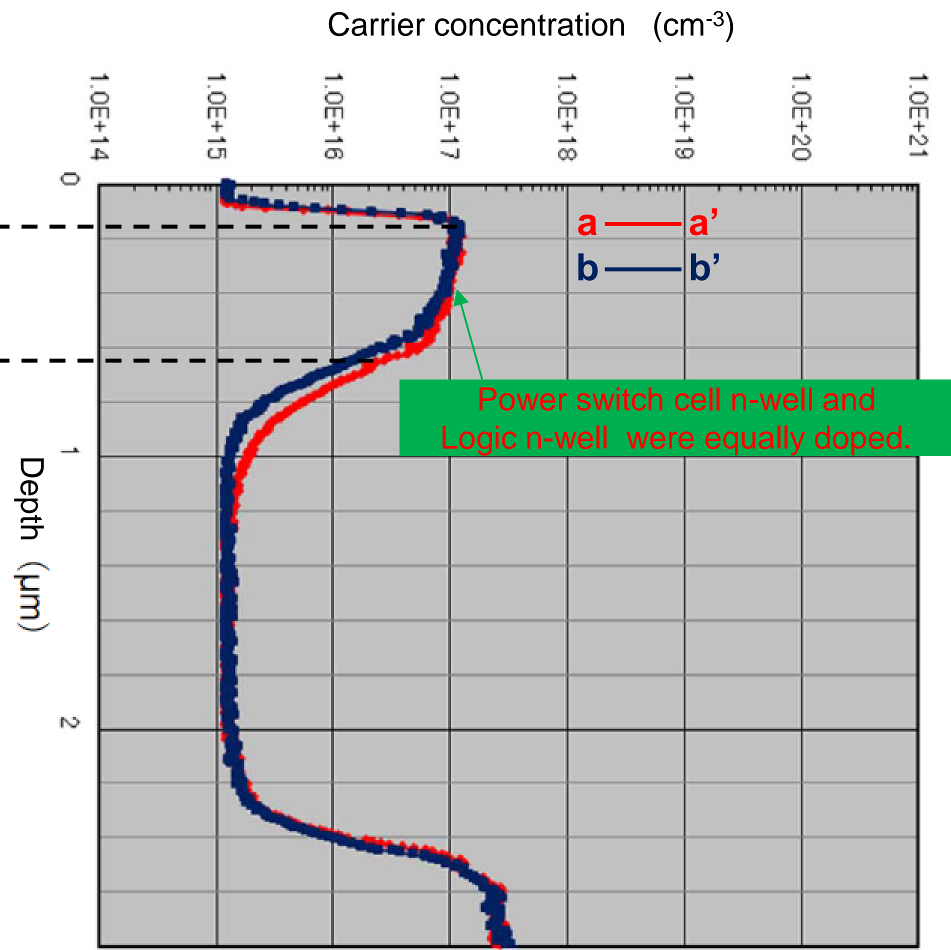


Fig. 5-10-5 a-a' line & b-b' line carrier concentration profile

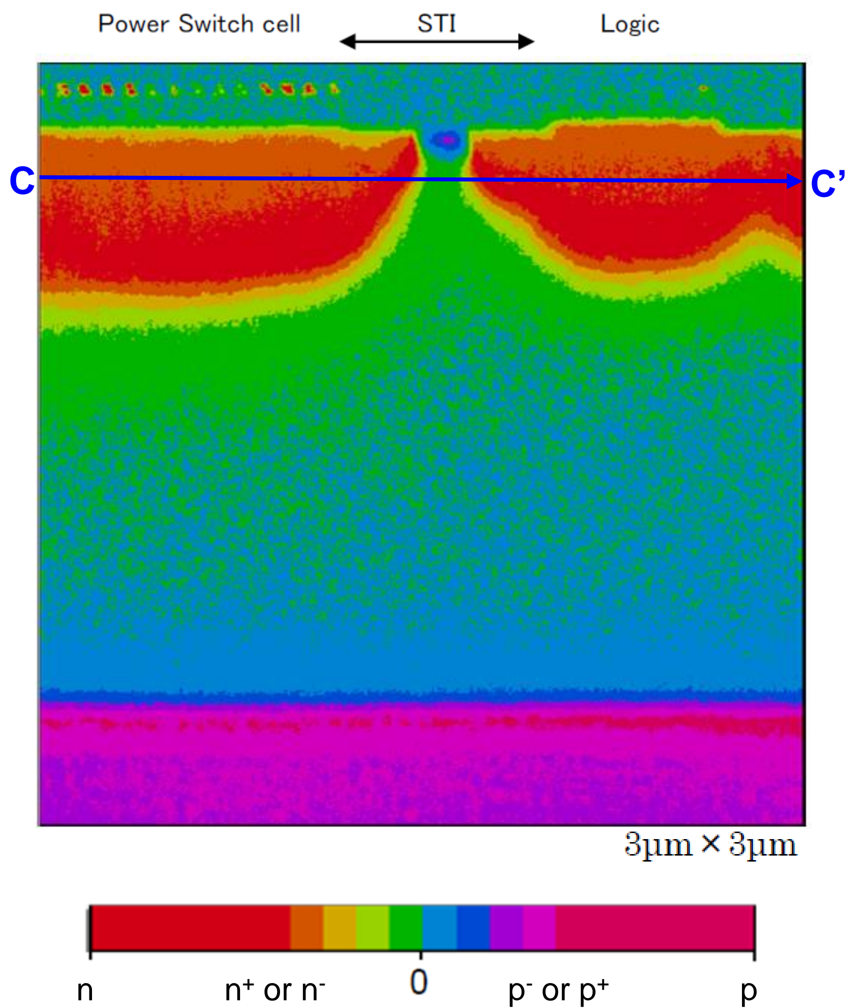


Fig. 5-10-6 SCM dC/dV image

C
C'
N-well didn't continue between power switch cell and logic area.
Carrier concentration (cm-3)
1.0E+20
1.0E+19
1.0E+18
1.0E+17
1.0E+16
1.0E+15
1.0E+14
0
1
2
3
Depth (μm)

Fig. 5-10-7 c-c' line carrier concentration profile

1−3. Mask Sequence (1P8M CMOS Logic)

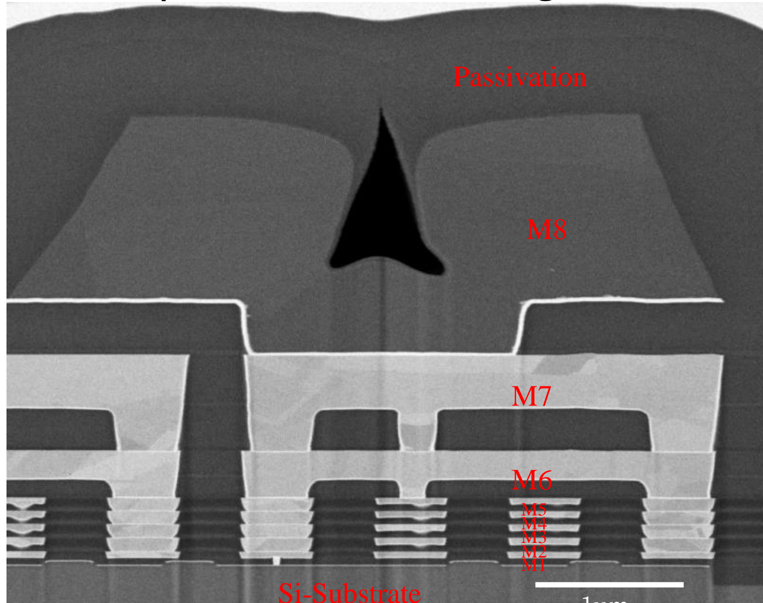


Figure.1-2-1 General Device Structure

Table.1-3 **Mask Sequence and number of masks**

Mask Sequence	Number of Masks
Isolation (STI)	3
Well formation	2
Gate	1
LDD formation	2
S/D formation	2
Salicide protection	1
Contact	1
Metal wiring	8
Via	7
Pad opening	1
Total	28

Typical Mask sequence(1P8M CMOS)

- ISO1; Definition of thin oxide for device
- ISO2; Definition of reverse thin oxide
- PW; Definition of P-well
- NW; Definition of N-well
- ISO3; Definition of thick oxide for device
- Gate; Definition of Gate Poly-Si
- LDD1; Definition of LDD (RV)
- LDD2; Definition of LDD (HV)
- PP; Definition of P+
- NP; Definition of N+
- SP; Definition of Salicide protection
- C; Definition of Contact
- M1; Definition of M1
- V1; Definition of Via1
- M2; Definition of M2
- V2; Definition of Via2
- M3; Definition of M3
- V3; Definition of Via3
- M4; Definition of M4
- V4; Definition of Via4
- M5; Definition of M5
- V5; Definition of Via5
- M6; Definition of M6
- V6; Definition of Via6
- M7; Definition of M7
- V7; Definition of Via7
- M8; Definition of M8
- Pad; Definition of bonding pad

Appendix 1-2 Process information

Table 5-3 Constituent Materials and Process tech summary

Level	Constituent Materials	Process
Passivation	SiN/SiO	P-CVD
M12 / Via11	Copper with Ta based materials barrier	Via-first dual damascene process CMP, EP, PVD, CVD
M12 IMD / M12-M11 ILD	SiOF / SiCN	P-CVD / Spin on
M11 / Via10	Copper with Ta based materials barrier	Via-first dual damascene process CMP, EP, PVD, CVD
M11 IMD / M11-M10 ILD	SiOF / SiCN	P-CVD / Spin on
M10 / Via9 ~ M2 / Via1	Copper with Ta based materials barrier	Via-first dual damascene process CMP, EP, PVD, CVD
M10 IMD / M10-M9 ILD ~ M2 IMD / M2-1 ILD	SiOC / SiO2/ SiCN	P-CVD / Spin on
M1 IMD	SiOC / SiO2/ SiCN	CVD
M1	Copper with Ta based materials barrier	Single damascene process
PMD	SiO2	CVD
Contact	W with TiN/Ti barrier	CVD, PVD, CMP
Silicide	NiPtSi	PVD, Salicide process
Sidewall spacer	SiO2, SiN sidewall spacers	CVD
Source/ Drain	Embedded SiGe in PMOS source/ drain	
Gate/ Gate dielectric	NiPtSi/ Si/ Ti-based/ Hf-based	Gate first High-k Metal gate process
Isolation	SiO2	CVD, CMP, STI process

Table 5-3, wiring material and transistor forming material and estimation results of their formation process are summarized. These data are based on EELS and EDX analysis results in which it appears in Chapter 8.

ADF-STEM Image(M4)

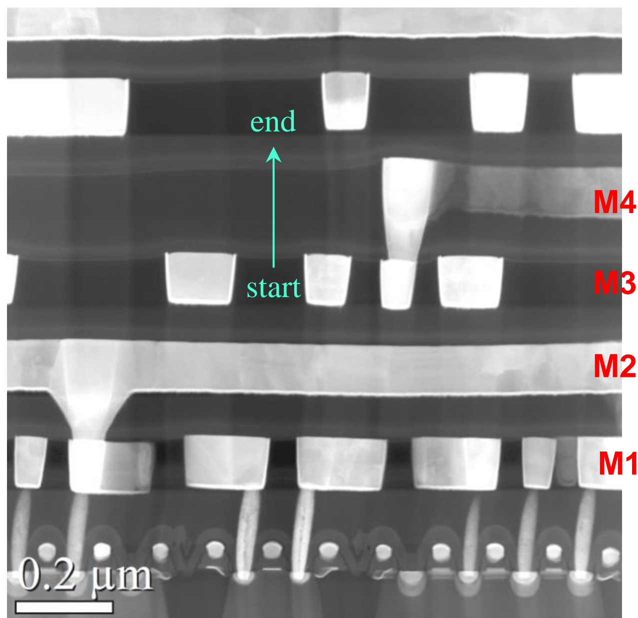
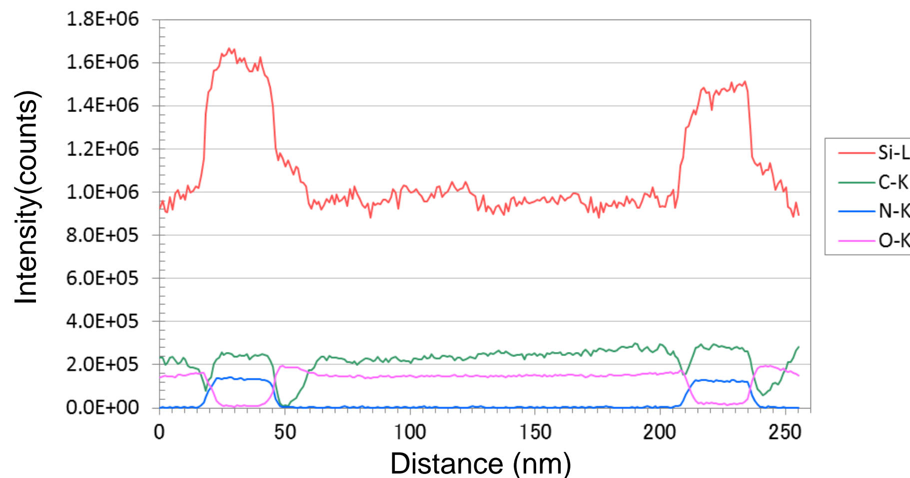


Fig. 8-1-2 EELS measurement position

Intensity



Composition

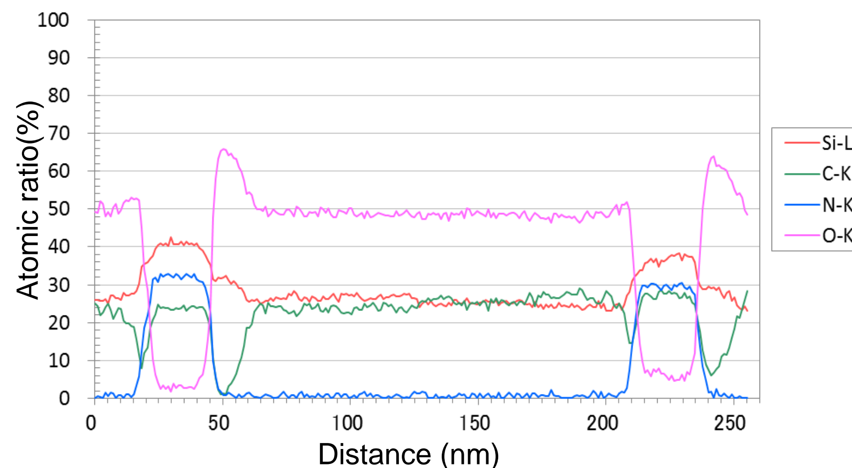
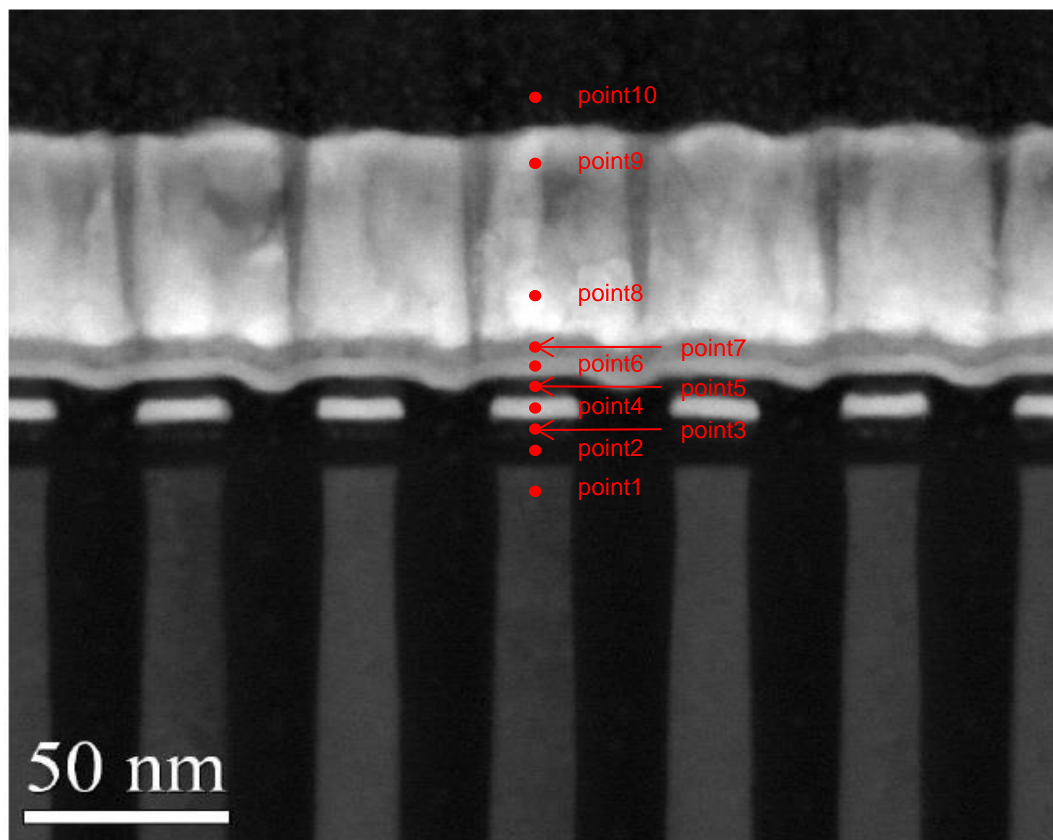
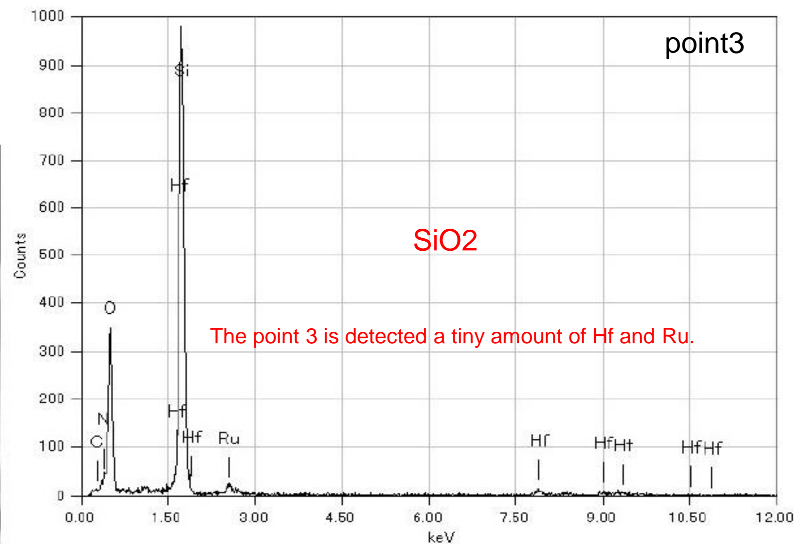


Fig. 8-1-3 M4 IMD and M4-M3 ILD EELS results

3. TEM EDX analysis- NAND Flash

Composition analysis (TEM EDX)





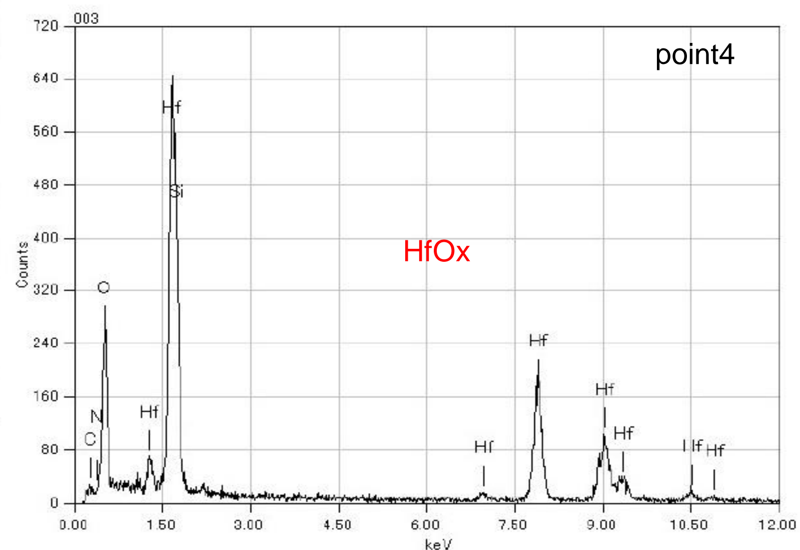


Fig. 3-1 NAND Flash Memory Cell TEM EDX analysis

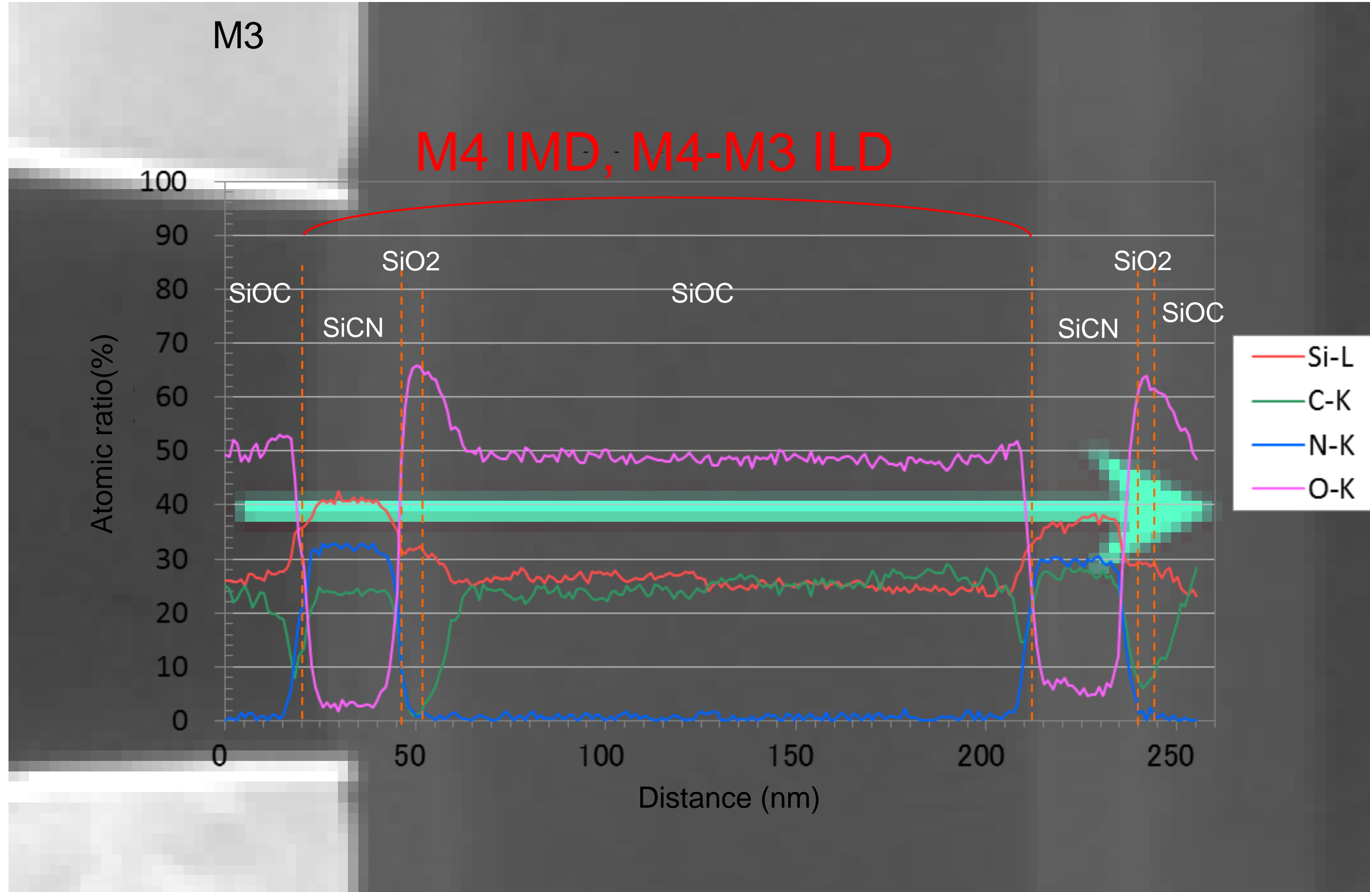
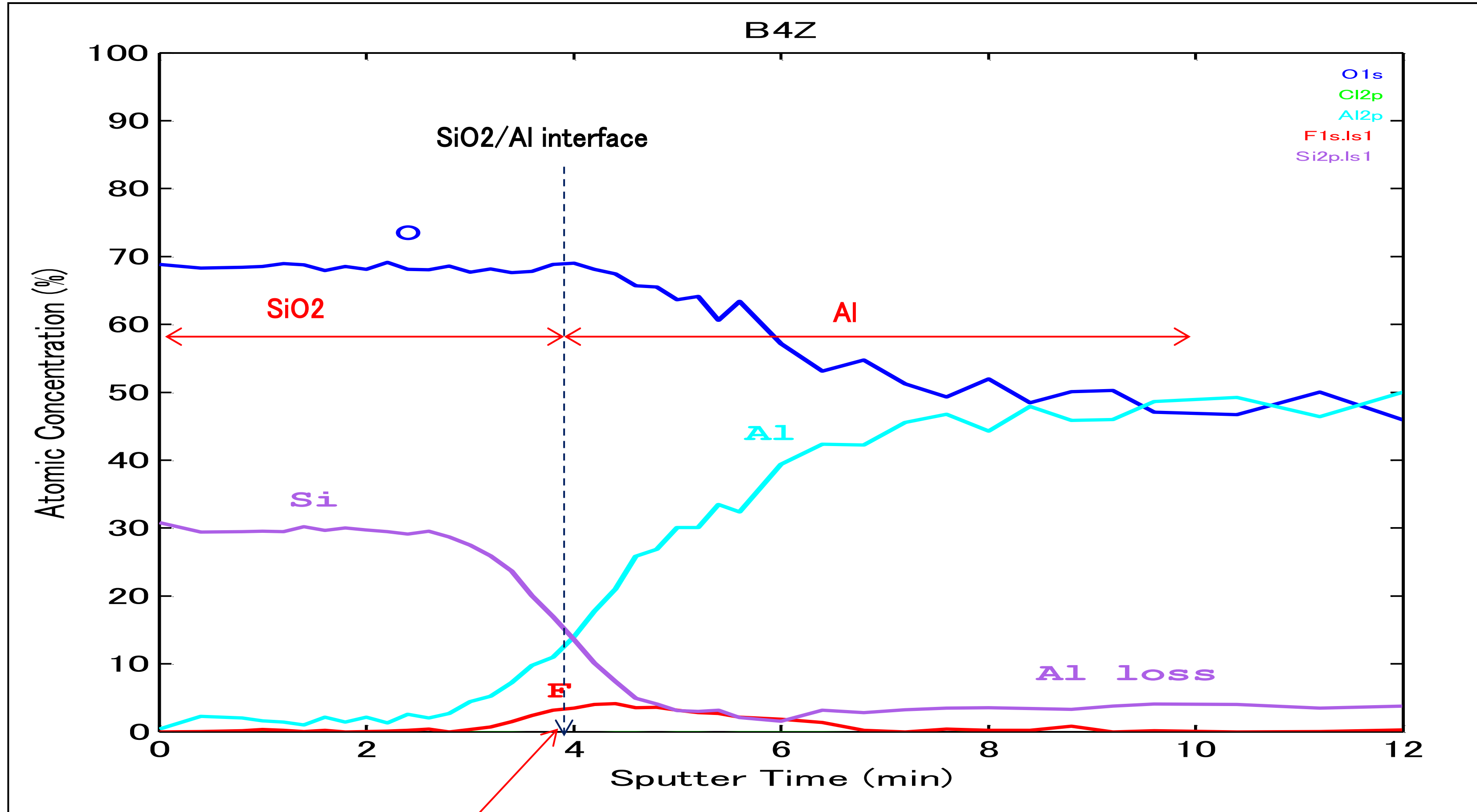


Fig. 8-1-4 M4 IMD and M4-M3 ILD EELS results Summary

Appendix 6 ESCA(XPS) analysis

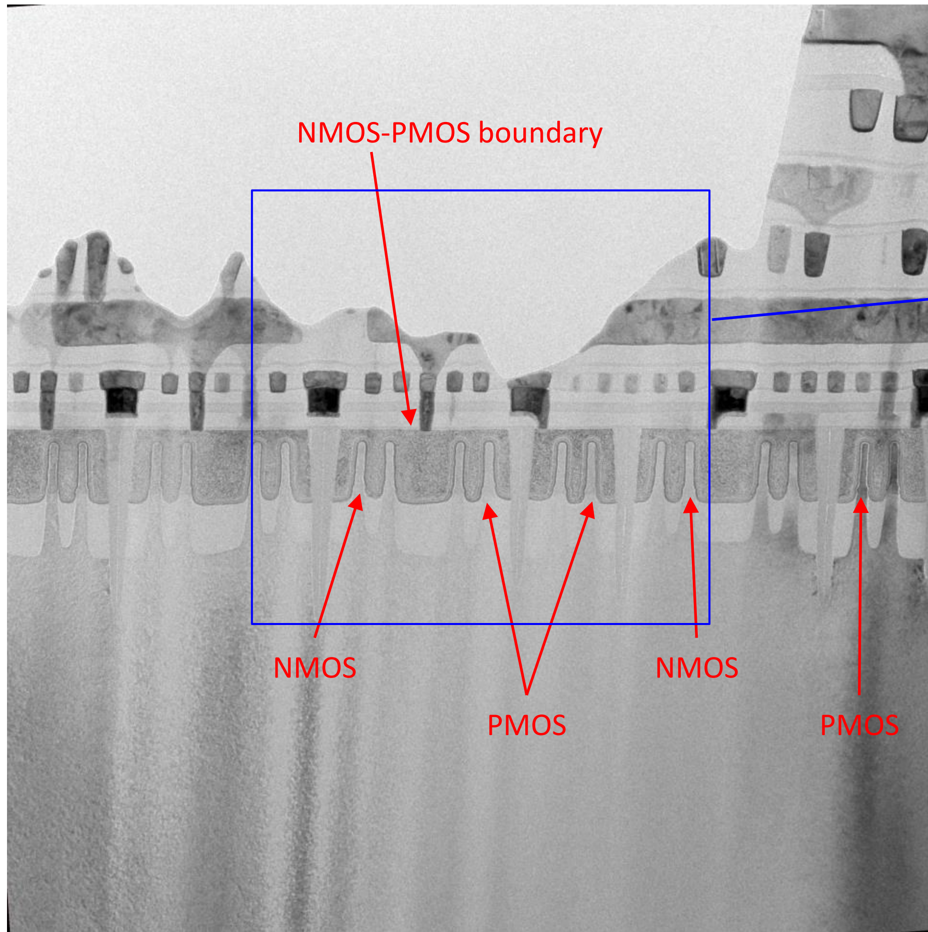


Fluorine at SiO2/Al interface

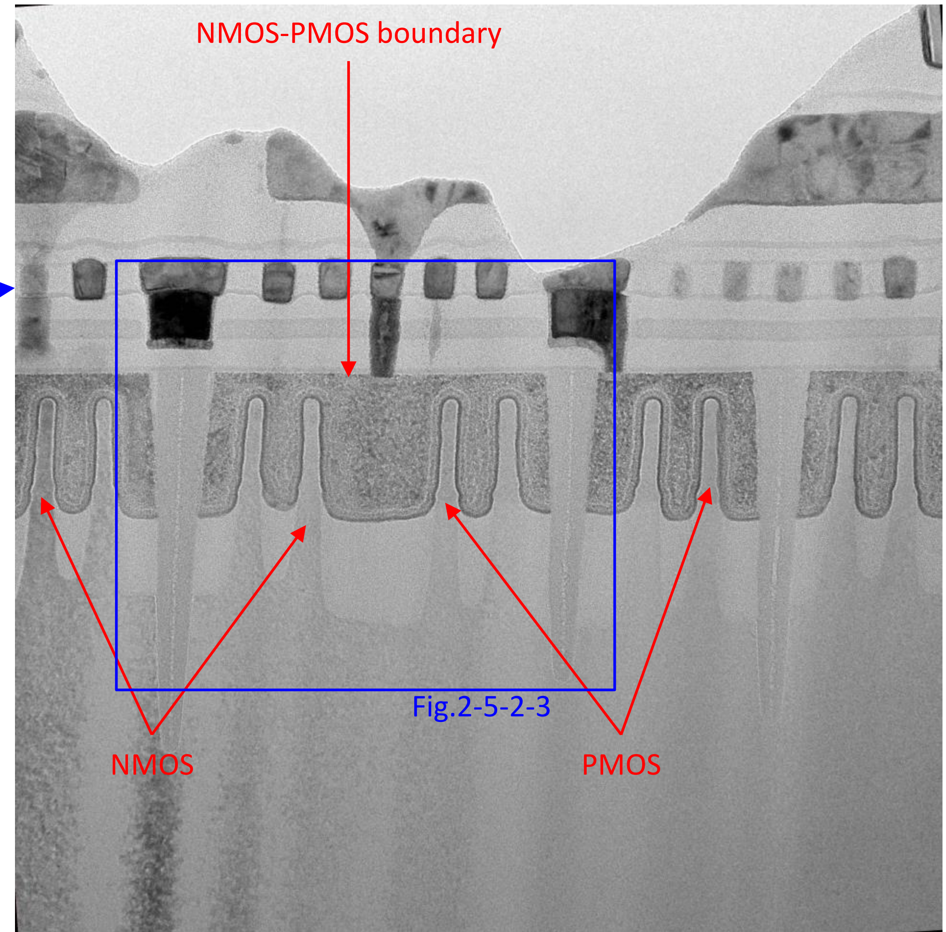
5nm processor structure analysis
Sample images

Core Logic TEM Cross-section Parallel to Gate Line

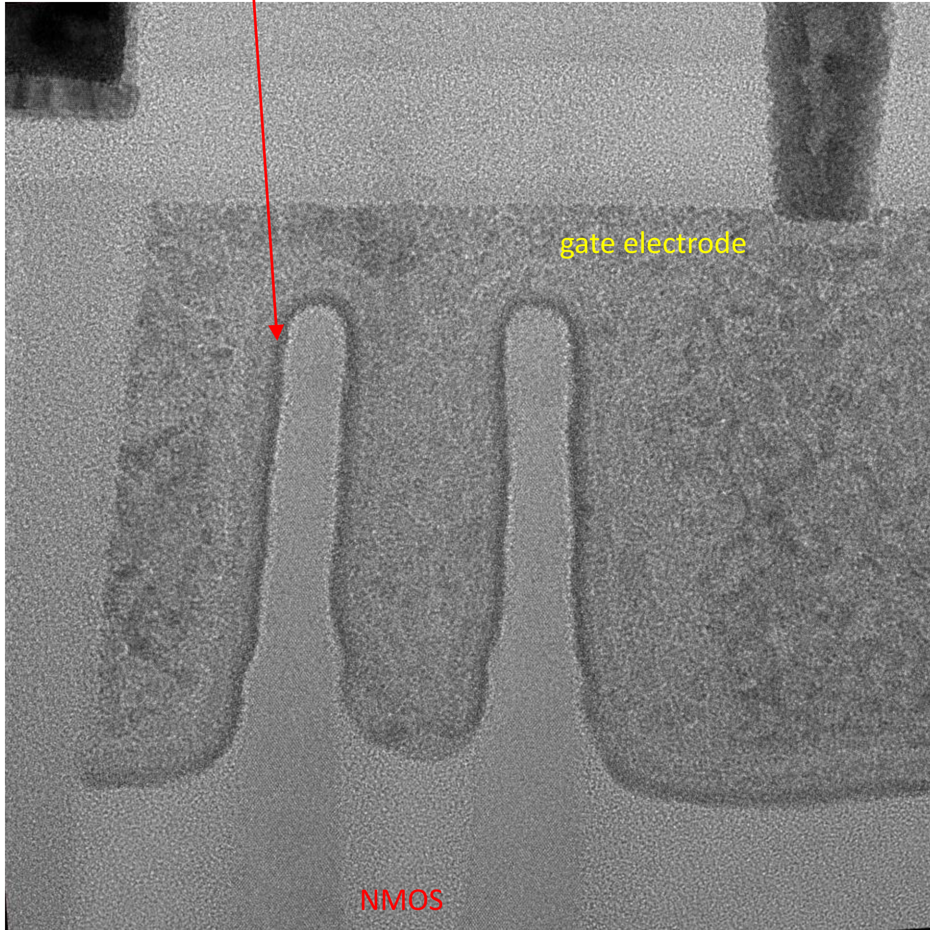
Gate Line



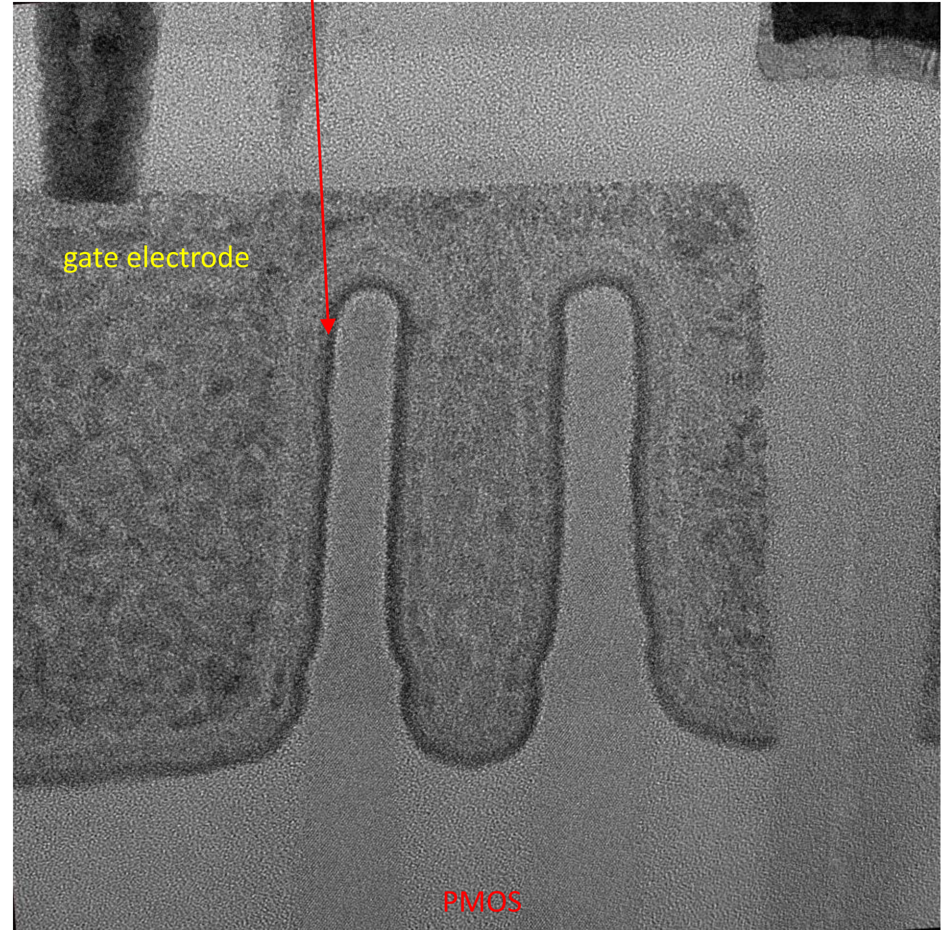
Cross sectional TEM image (gate electrode) 100nm



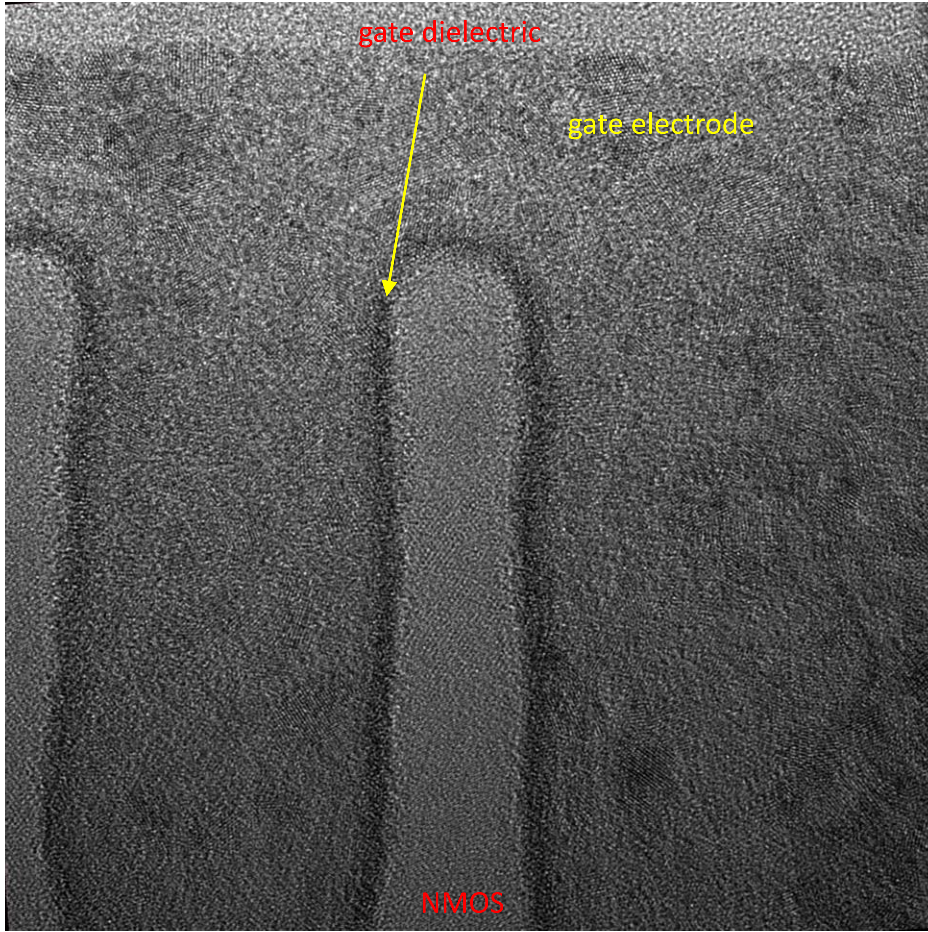
Cross sectional TEM image (gate electrode) 50nm



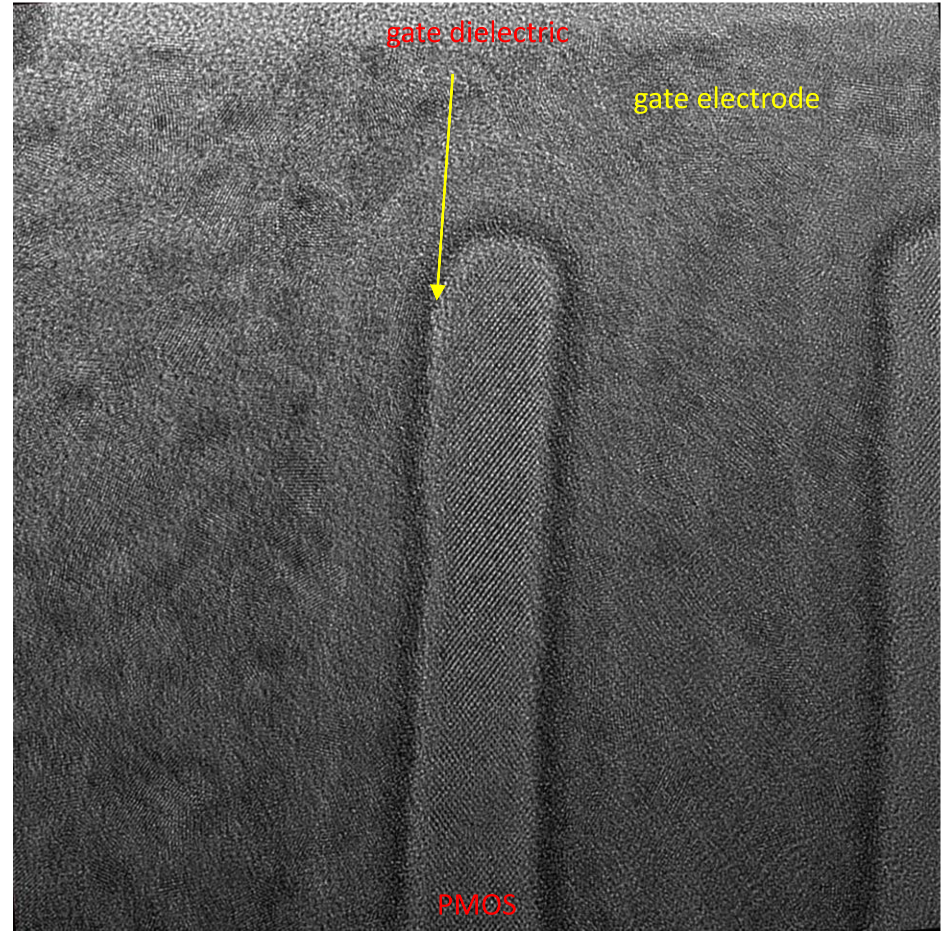
Cross sectional TEM image (gate electrode)



Cross sectional TEM image (gate electrode)



Cross sectional TEM image (gate electrode) 5nm

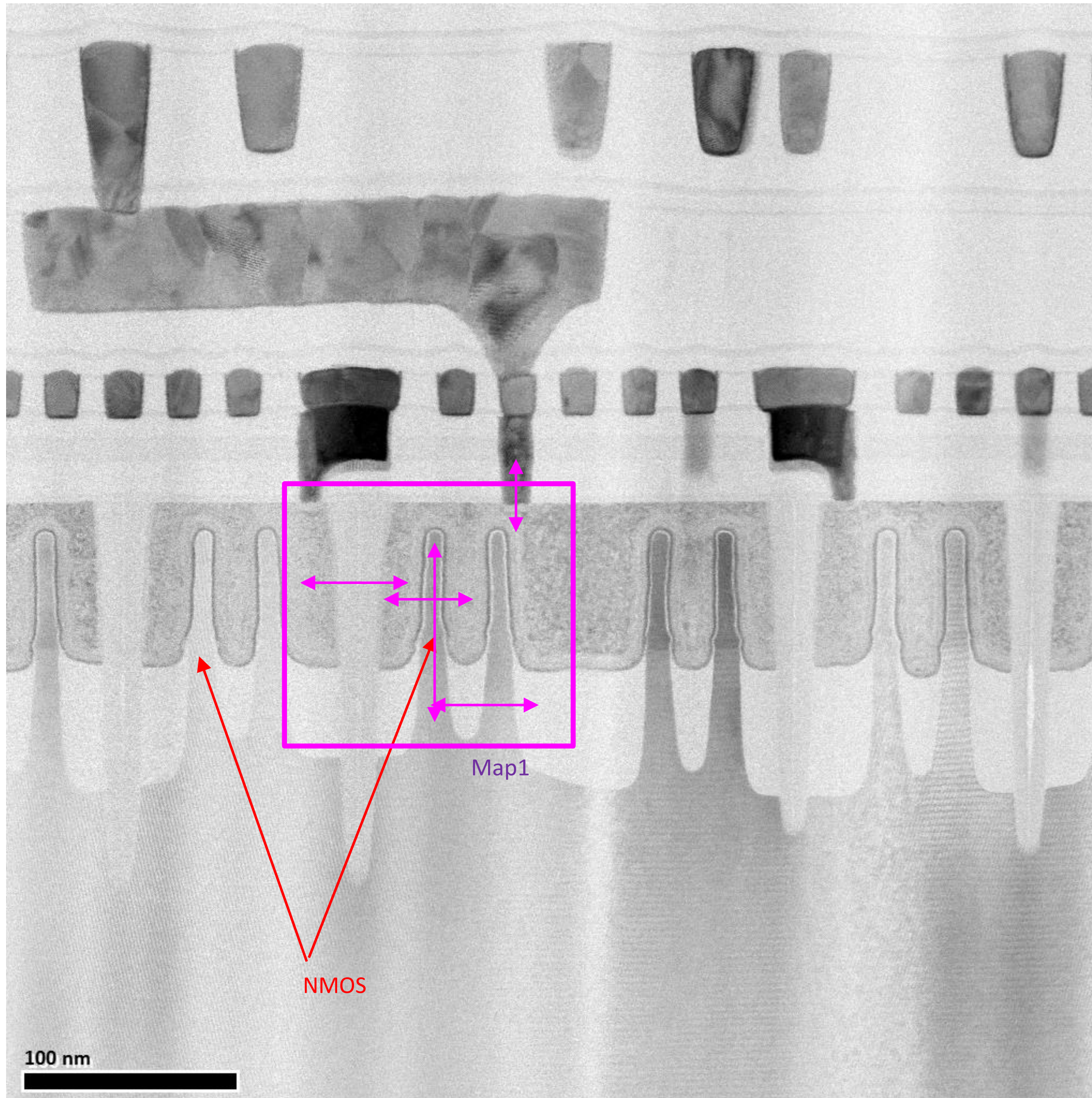


Cross sectional TEM image (gate electrode) 5nm

Note: The film thickness is calculated from the drawn scale.

Materials Analysis

Gate

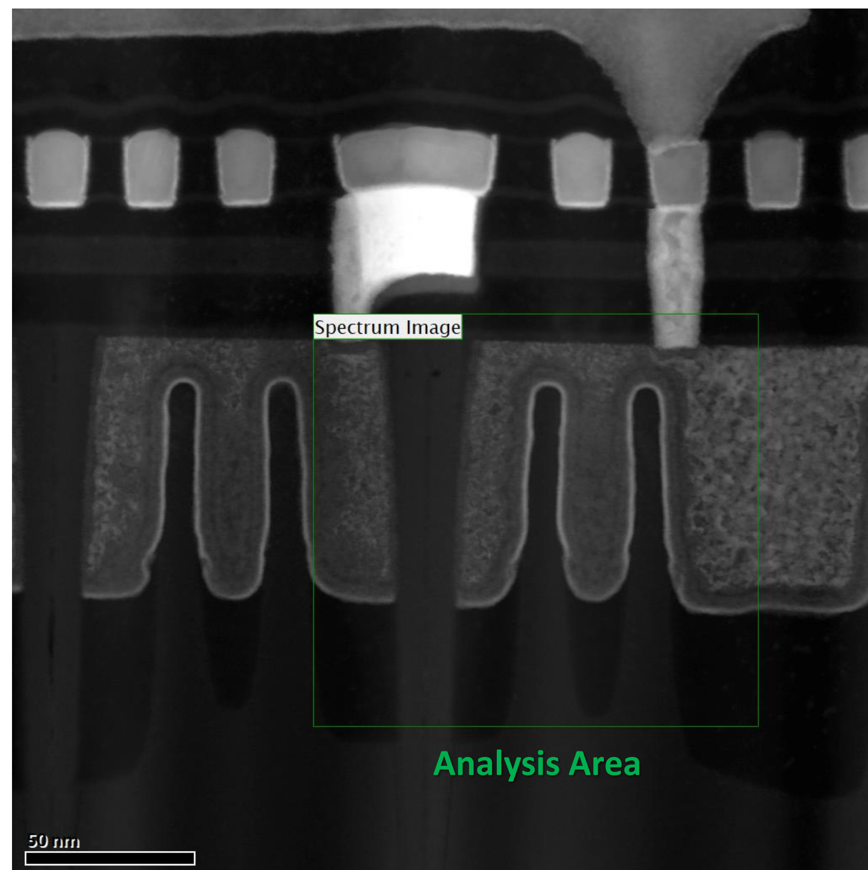


EELS Mapping Area

EELS line analysis position

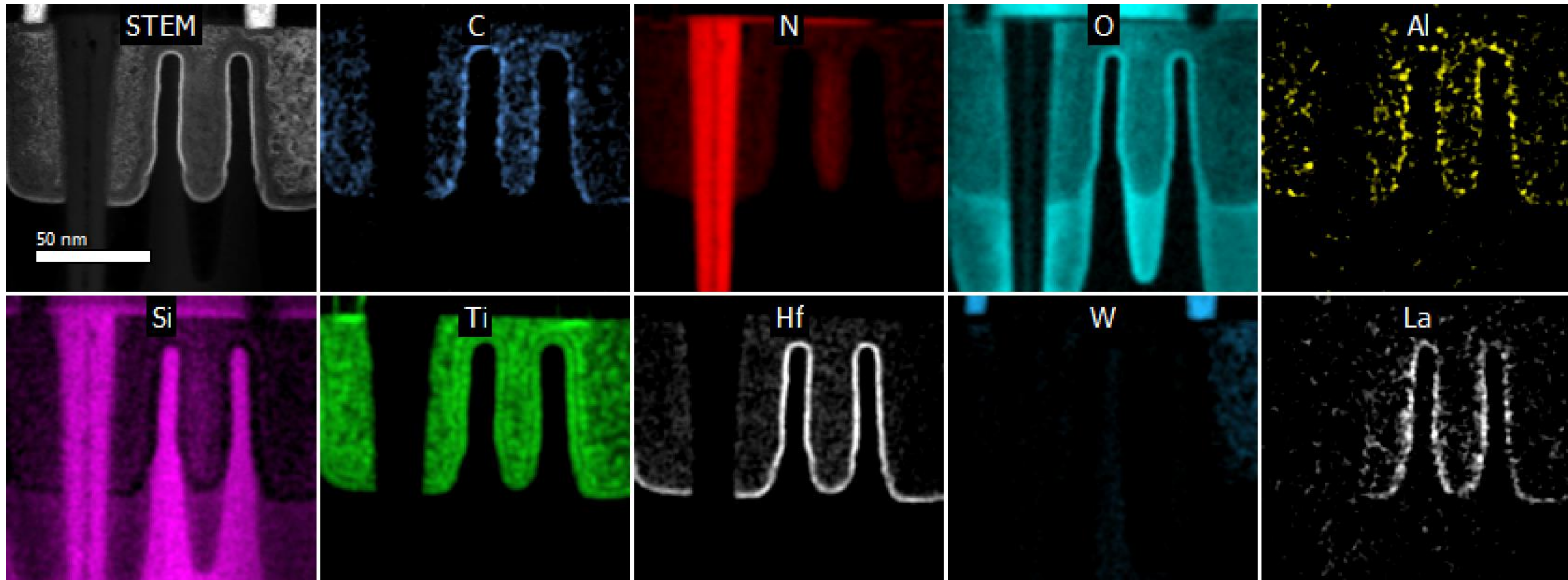
Fig. 2-6-1-1 Analysis Area

Map1



Analysis Area

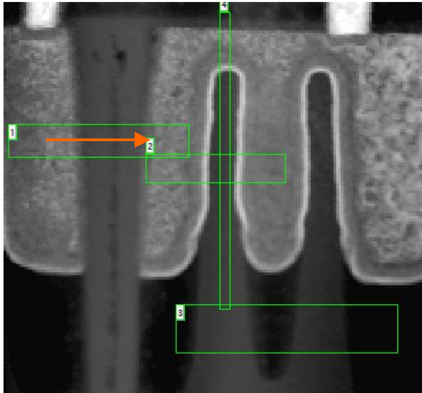
Map1



(Map contrasts are optimized to show element distributions, they are not directly proportional to actual abundances)

EELS Elemental Map

Map1
(line1)



realtive composition (at.%)

nm

C
N
O
Al
Si
Ti
Hf
W
La

EELS Analysis Result