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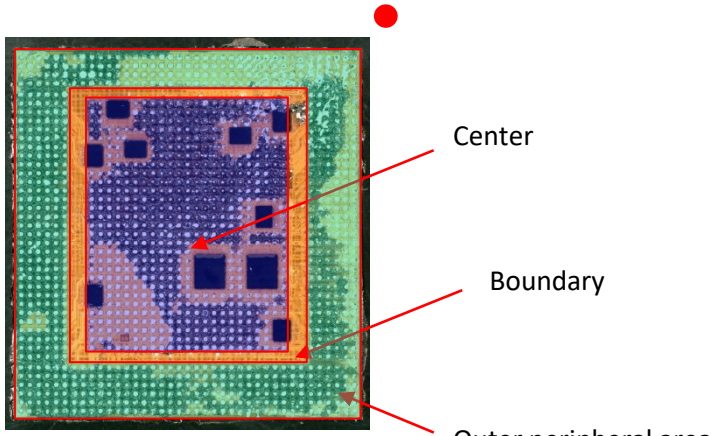
Note: LTEC can delver CAD format such as .mcm, pad, CR or ODB++.

Summary

Layer	Outer peripheral area	Boundary	Center
(Chip Bump)	-	-	-
RDL1	(Through INFO Via)	No pattern	Grid pattern power lines
RDL2	Signal Line	Signal Line	Power/GND
RDL3	Shield GND	Signal Line	Power/GND
RDL4	Signal Line	Signal Line	Power/GND
RDL5	UBM	No pattern	UBM
(Solder Ball)	-	-	-



Package Bottom view

1. Package

MLCC

Si Cap

Fig. 1-1 Package (Top view)

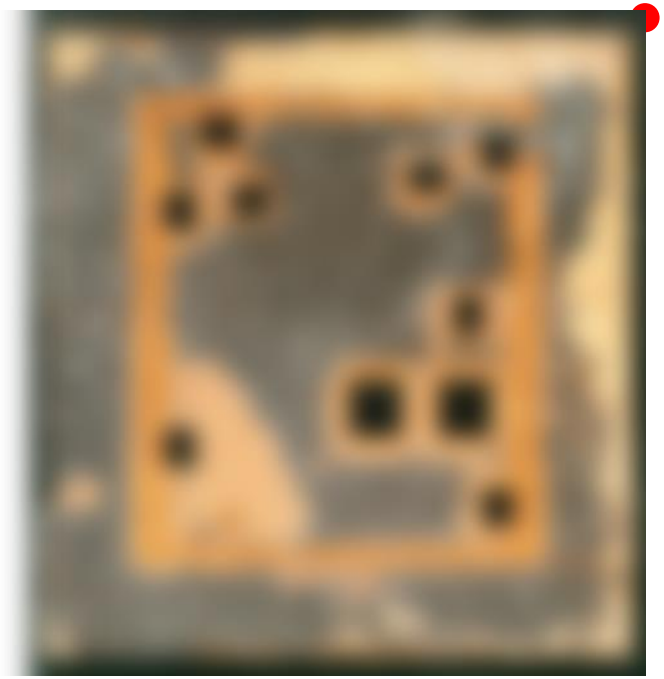


Fig. 1-2 Package (Bottom view)

● : 1st Pin Mark

2. RDL each layer

Fig. 2-1 RDL1 pattern (Bottom View)

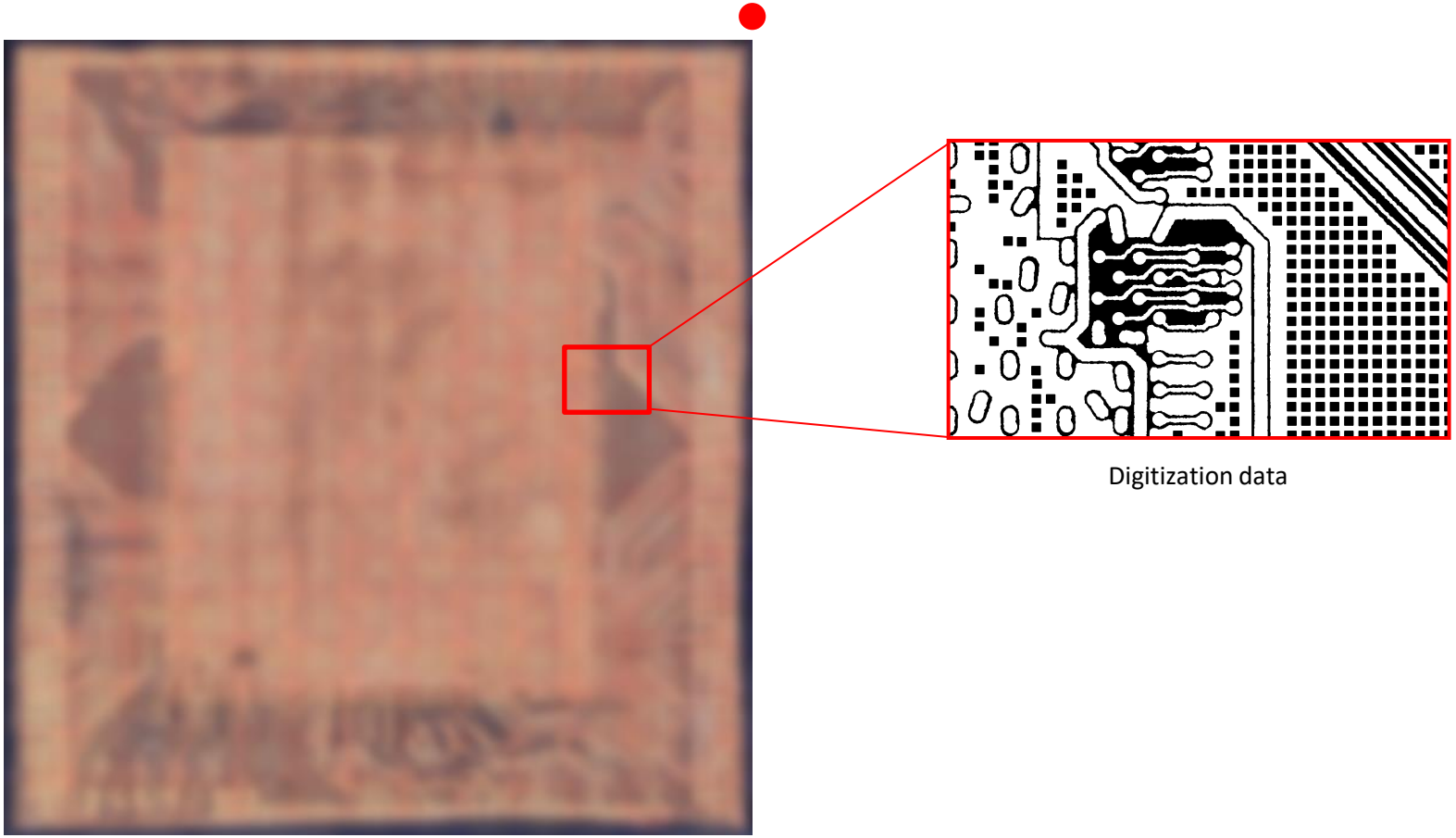


Fig. 2-2 RDL2 pattern (Bottom View)

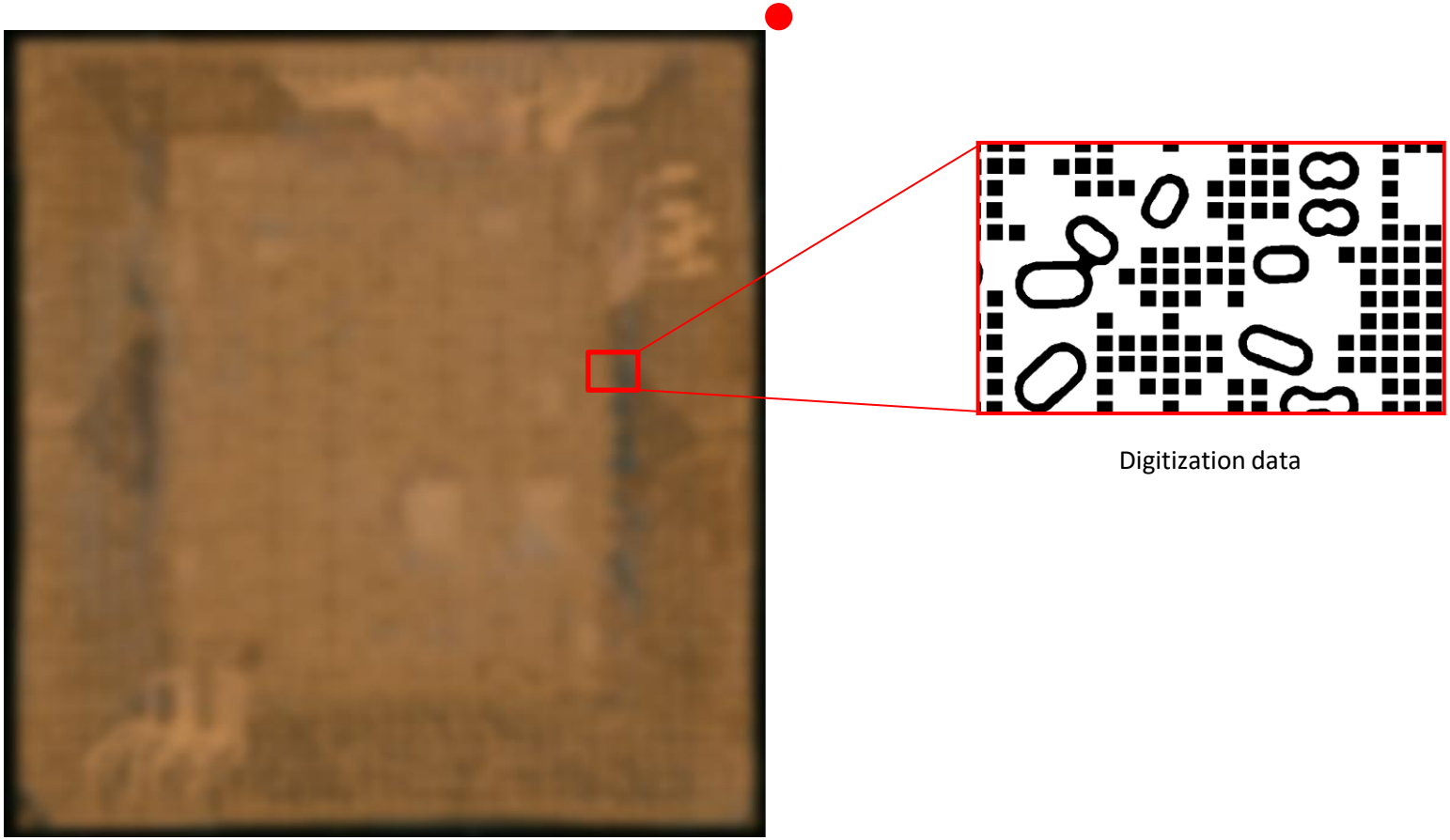


Fig. 2-3 RDL3 pattern (Bottom View)

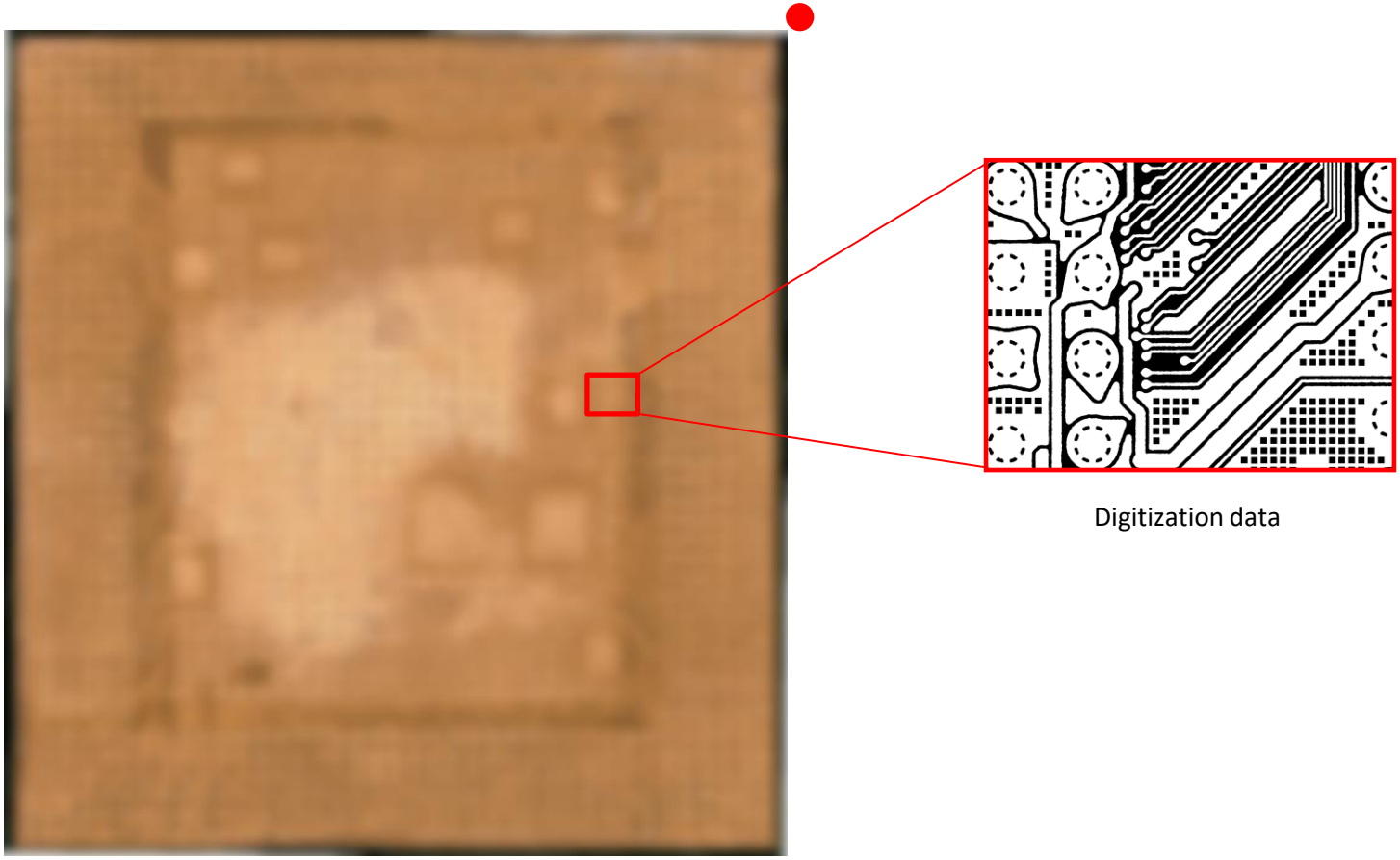
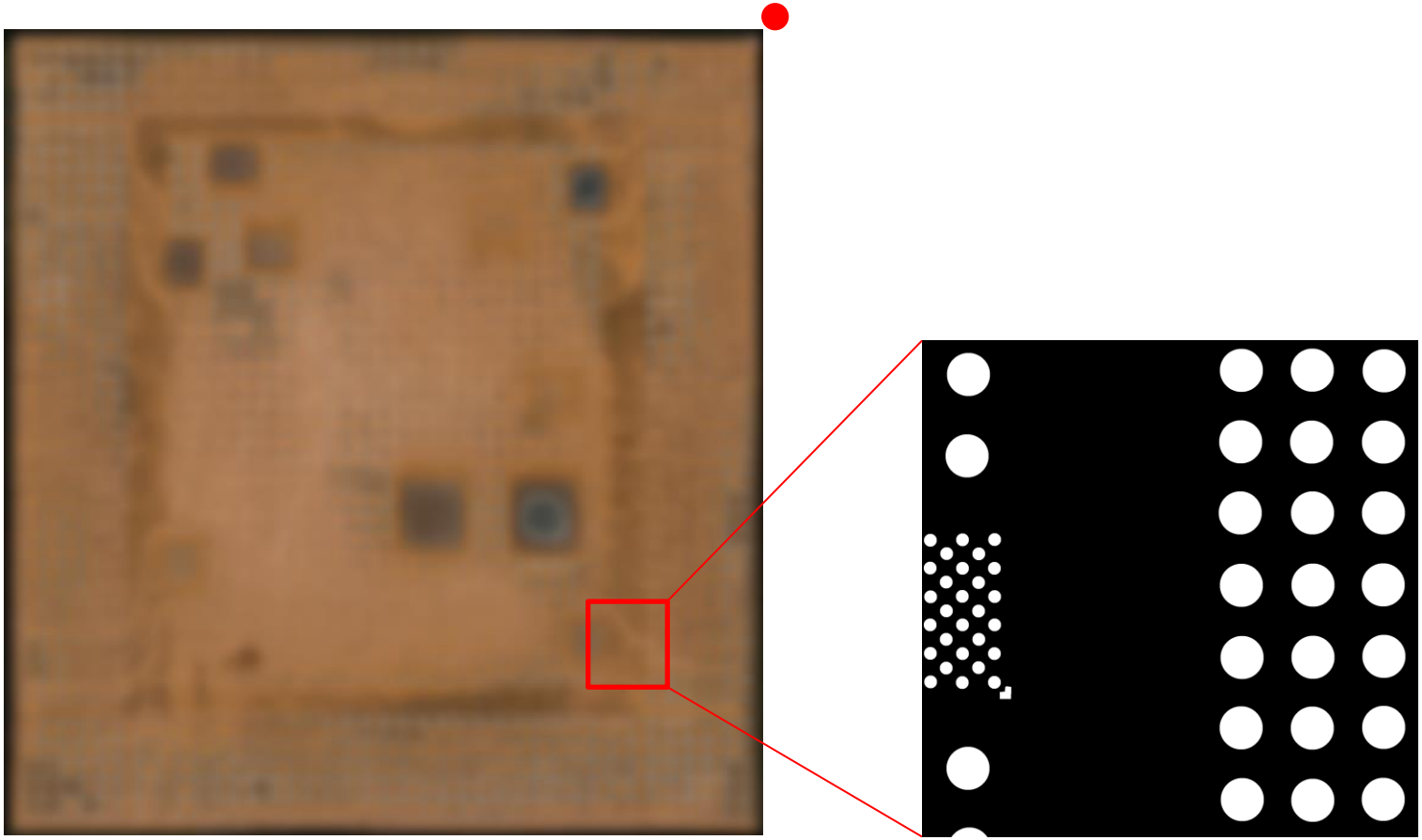


Fig. 2-4 RDL4 pattern (Bottom View)



Digitization data

Fig. 2-5 RDL5 pattern (Bottom View)

3. On-Package Capacitors

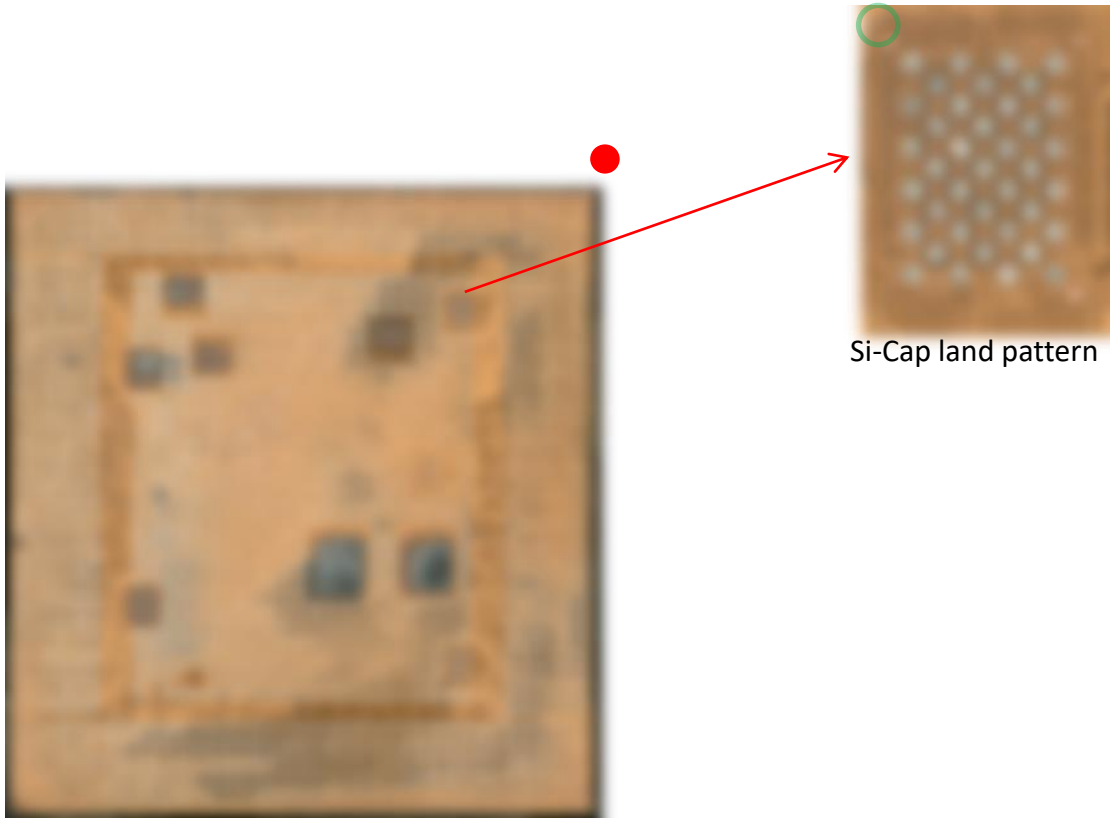


Fig. 3 Si-Cap Land pattern

4. Example of CAD format (ODB＋＋)

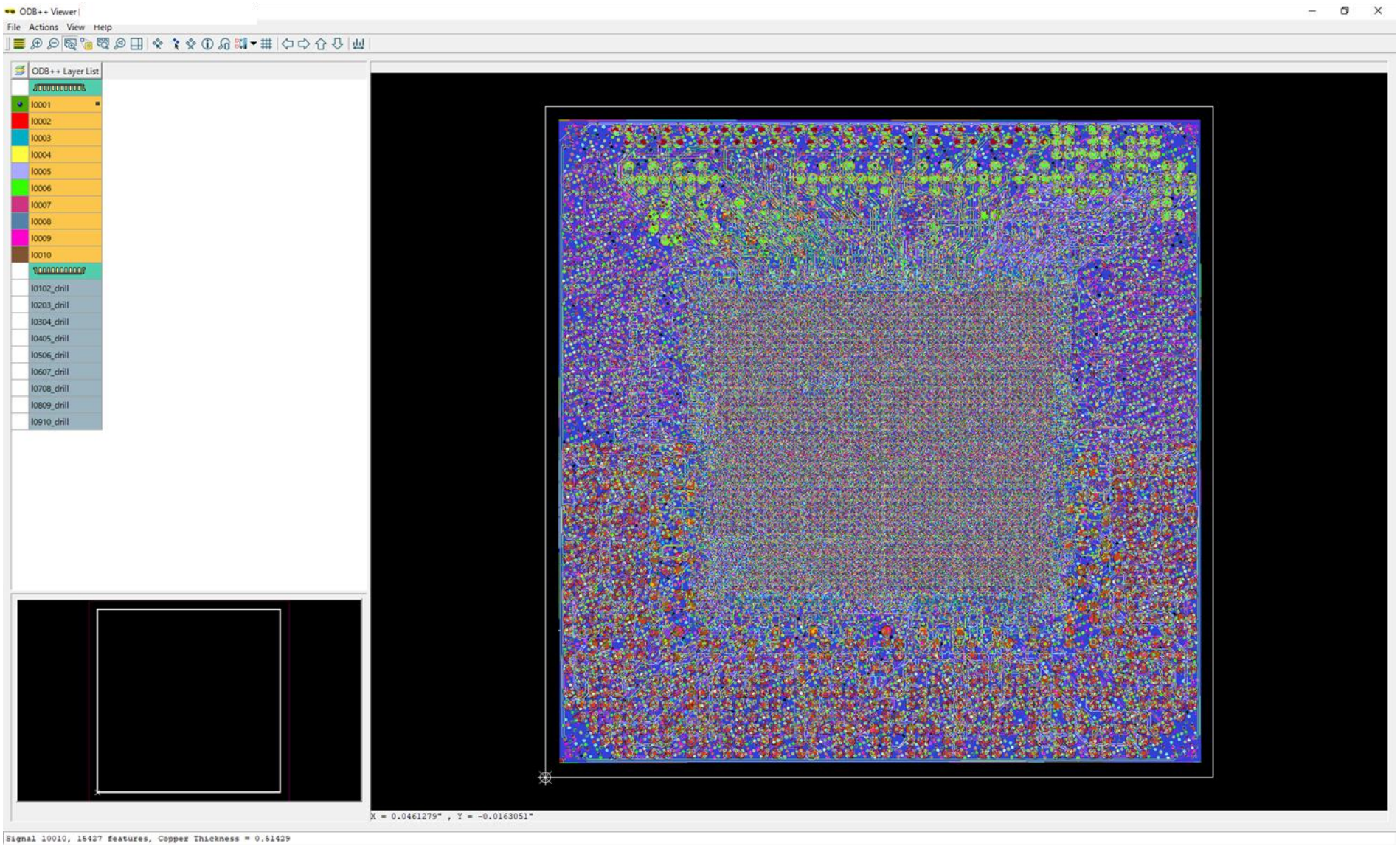


Fig. 4 ODB viewer