

# Coax-MIL Package Analysis of Intel Sapphire Rapids Xeon Gold 6430

**Purpose:**

Intel has used Air Core Inductors (ACIs) on package substrates to realize Fully Integrated Voltage Regulators (FIVR). The new product family, Sapphire Rapids, features a new coaxial magnetic composite core inductor called ([Coax MIL \[ coaxial magnetic inductor loops \]](#)), which dramatically improves its performance and quality factor, resulting in reduced ripple current and increased efficiency of the fully Integrated Voltage Regulator (FIVR). This report will focus on planar magnetic composite cores.

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LTEC Corporation

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**Summary:**

1. The package substrate has 22 layers, and the Coax MIL is implemented using the core layer
2. Coax MIL is an inductor that uses Through Hall (TH).The inside of TH is consist of non-magnetic material, and the area around TH is consist of the magnetic material.
3. The schematic on the right shows a simplified connection between the CPU Die and Coax MIL.

Connection to Die



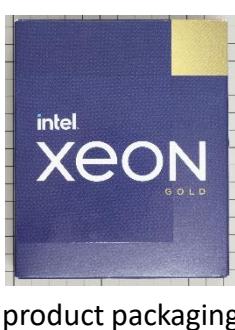
A2

A1

Connection to Die



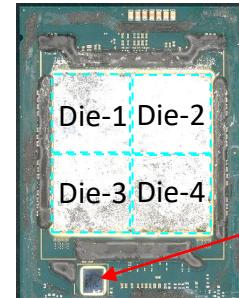
B



product packaging



Package

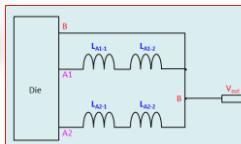


Substrate

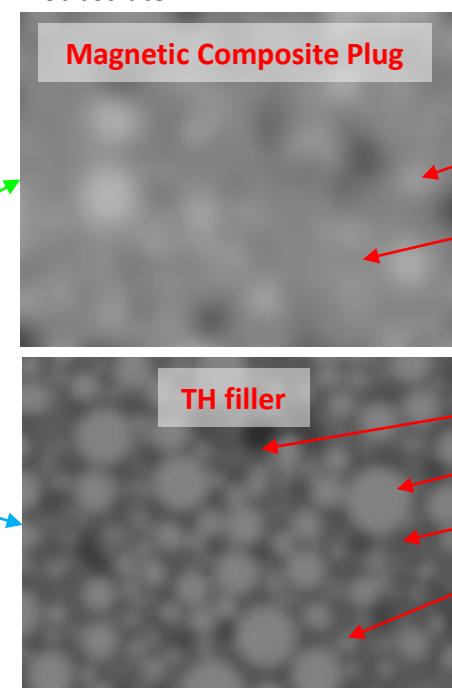
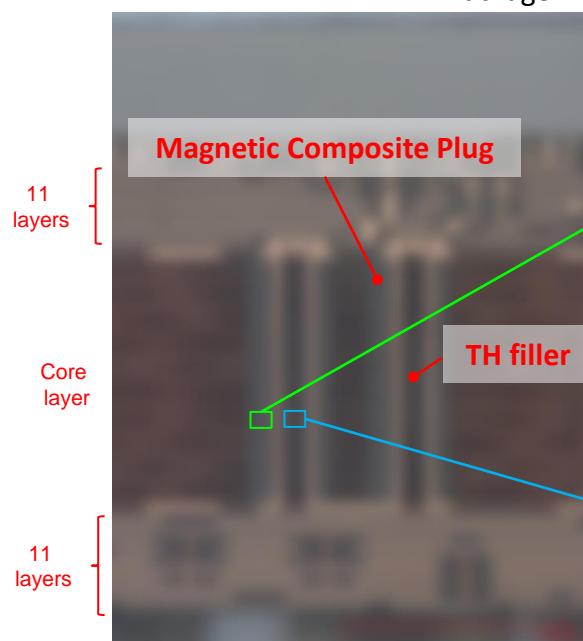
programmable  
logic devices  
[ PLDs ]

Coax MIL

$L_{A1-1}$

 $L_{A2-1}$  $L_{A1-2}$  $L_{A2-2}$ 

Coax MIL Pattern



TH : Through Hole

## 1. Product Overview



Fig. 1-2 Image of inner case

Fig. 1-1 Image of product packaging

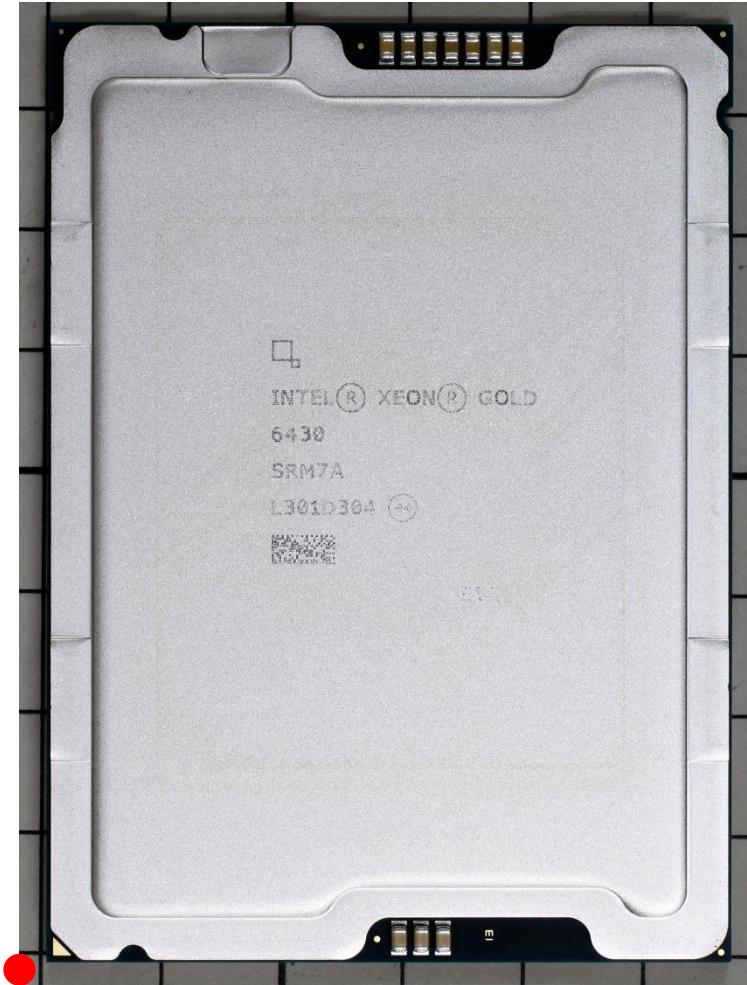


Fig. 1-3 Image of Package (Front)

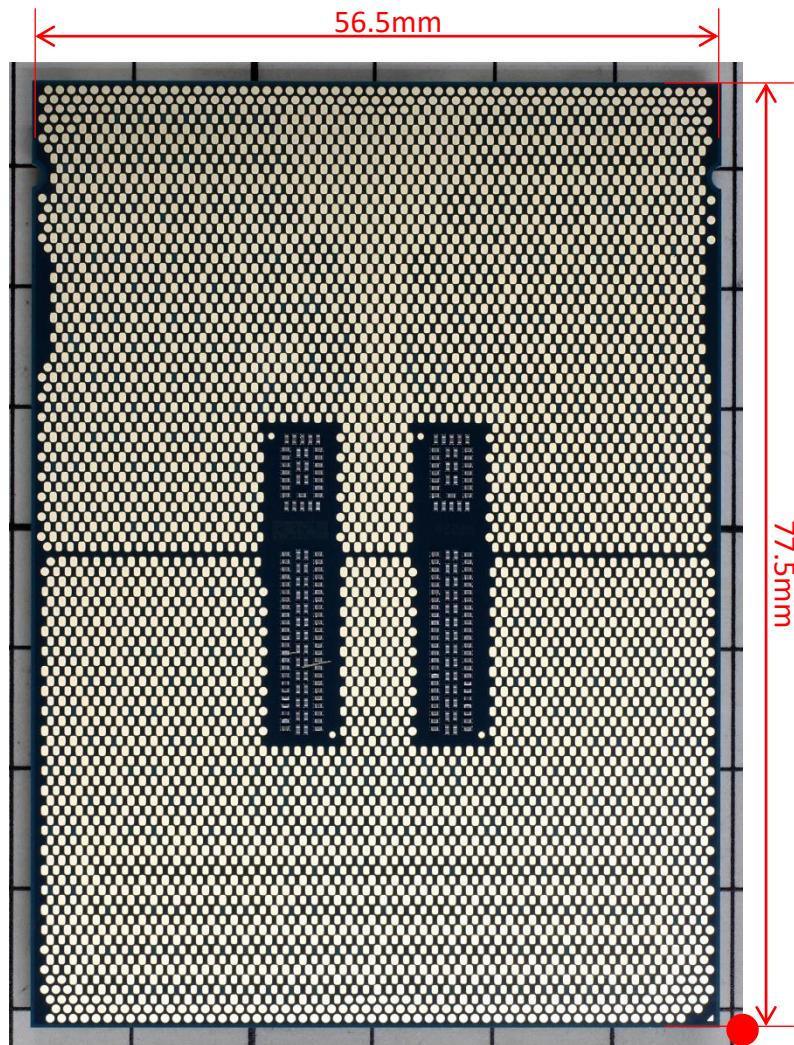


Fig. 1-4 Image of Package (Back)

## 2. X-ray observation

Array of Coax MIL

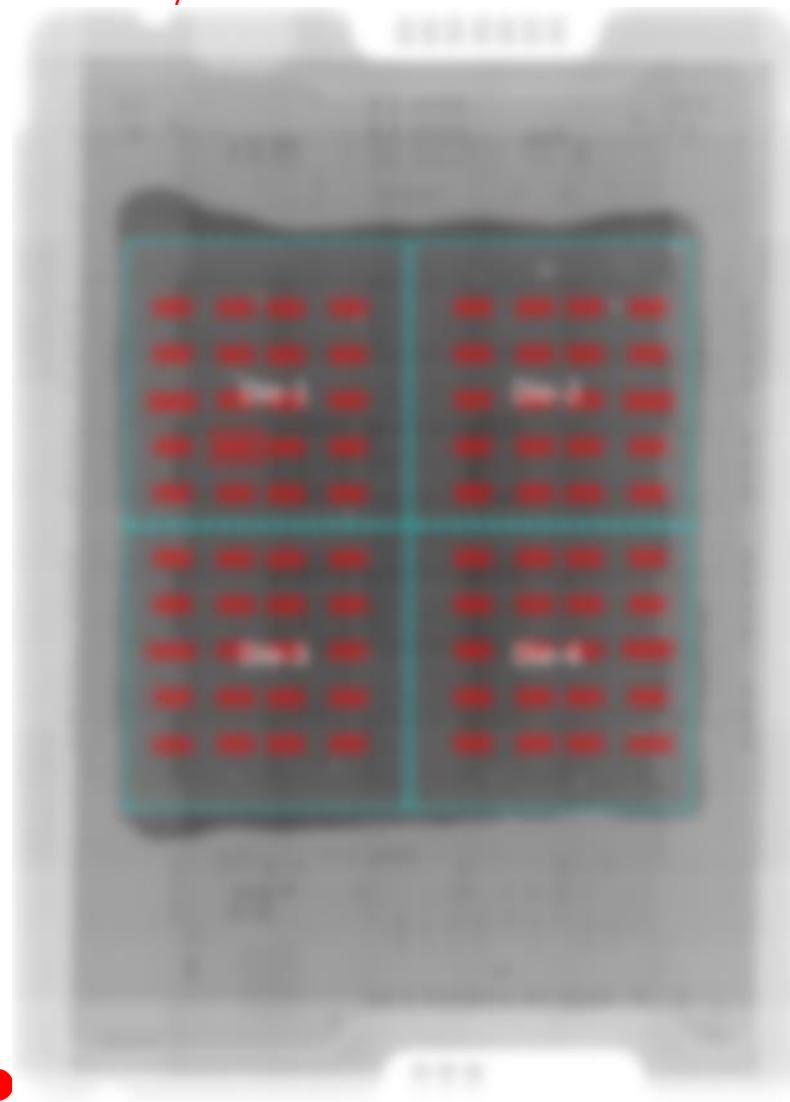


Fig. 2-1 X-ray image of the Package

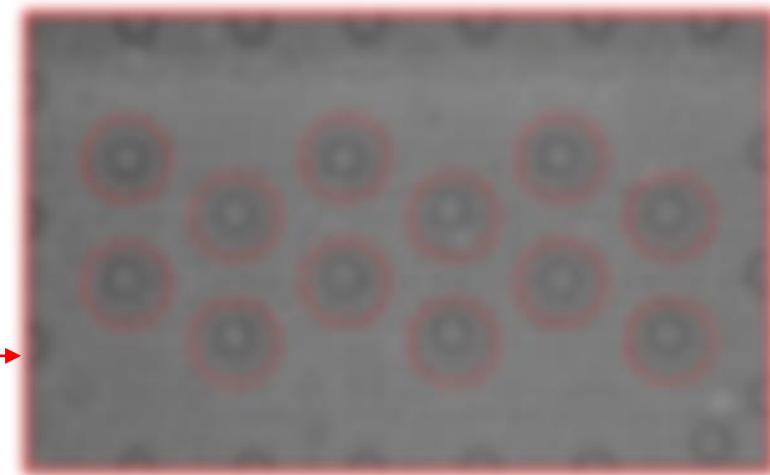


Fig. 2-2 X-ray image of an array of Coax MIL inductor

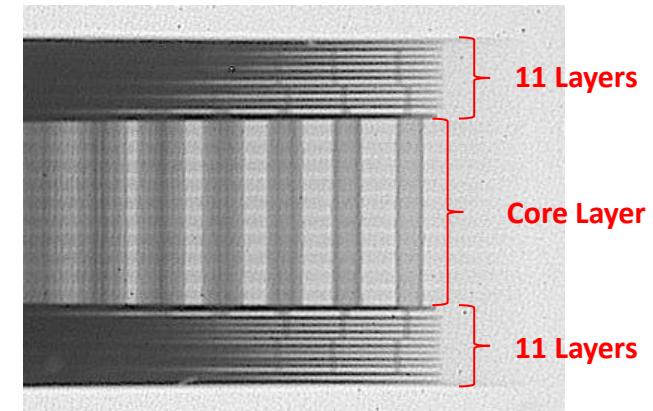


Fig. 2-3 Checking the number of interconnect layers

### 3. Substrate after heat sink removal



Fig. 3-1 Heat sink removal

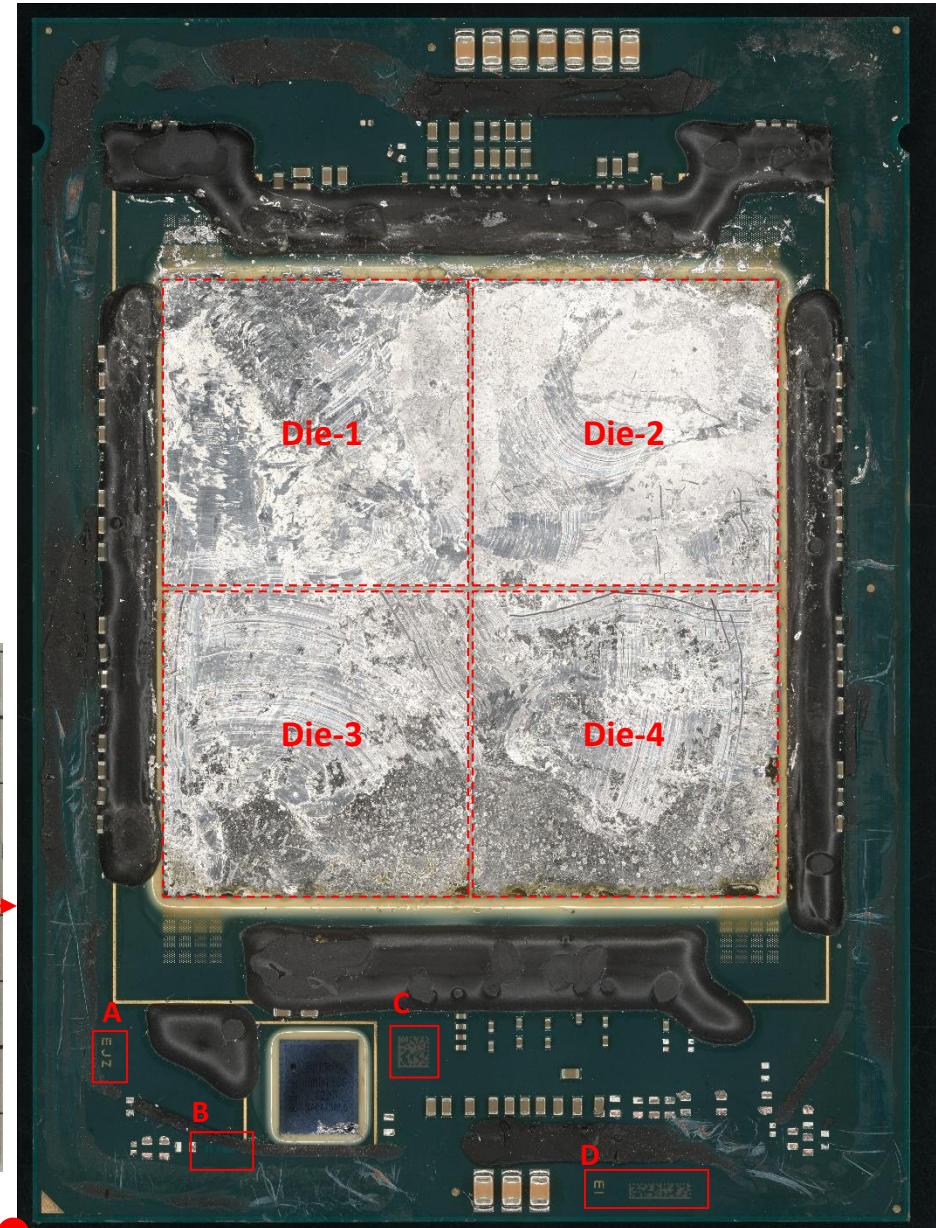


Fig. 3-2 Substrate after heat sink removal

Substrate wire tracing area:

Array of Coax MIL

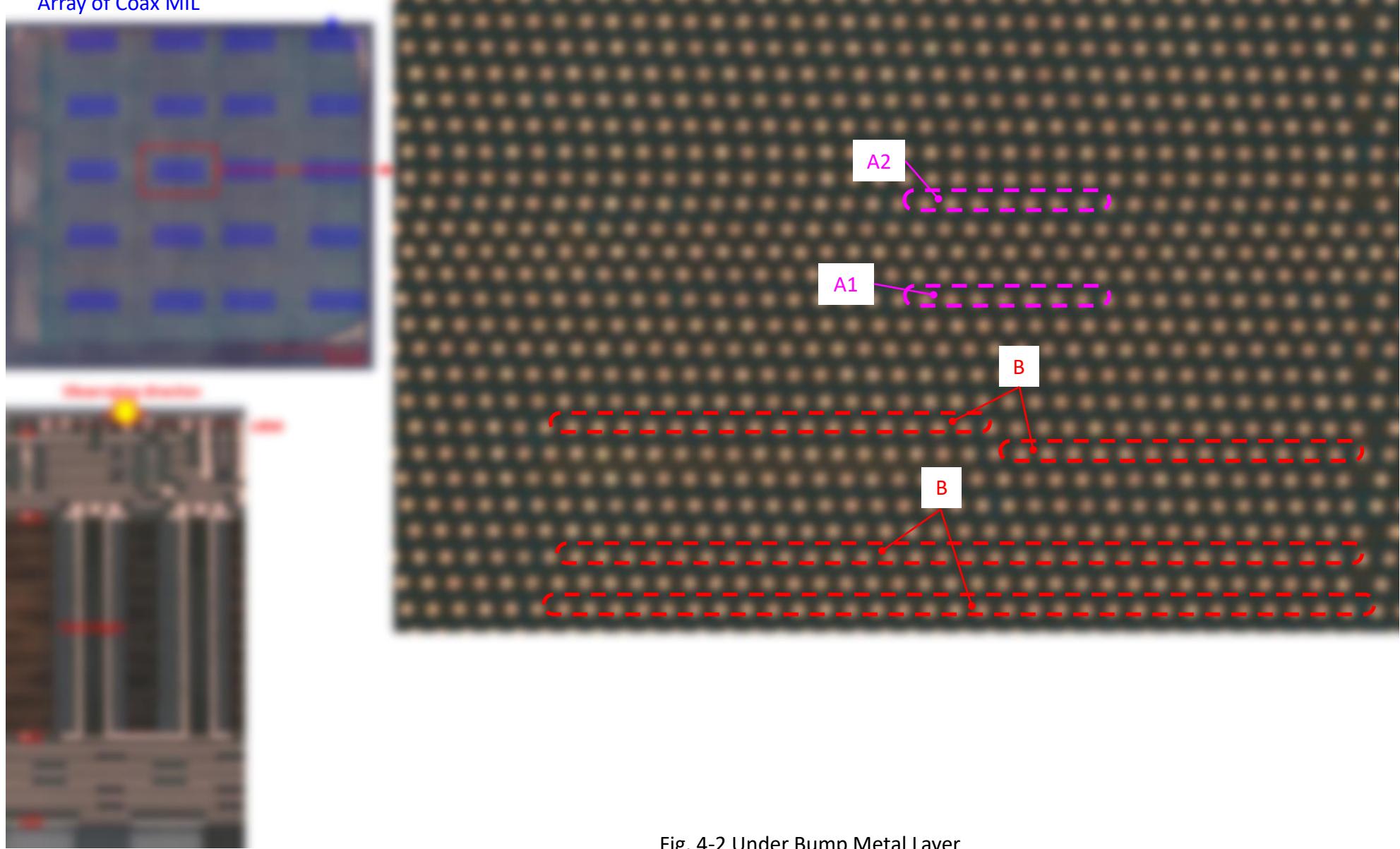


Fig. 4-2 Under Bump Metal Layer

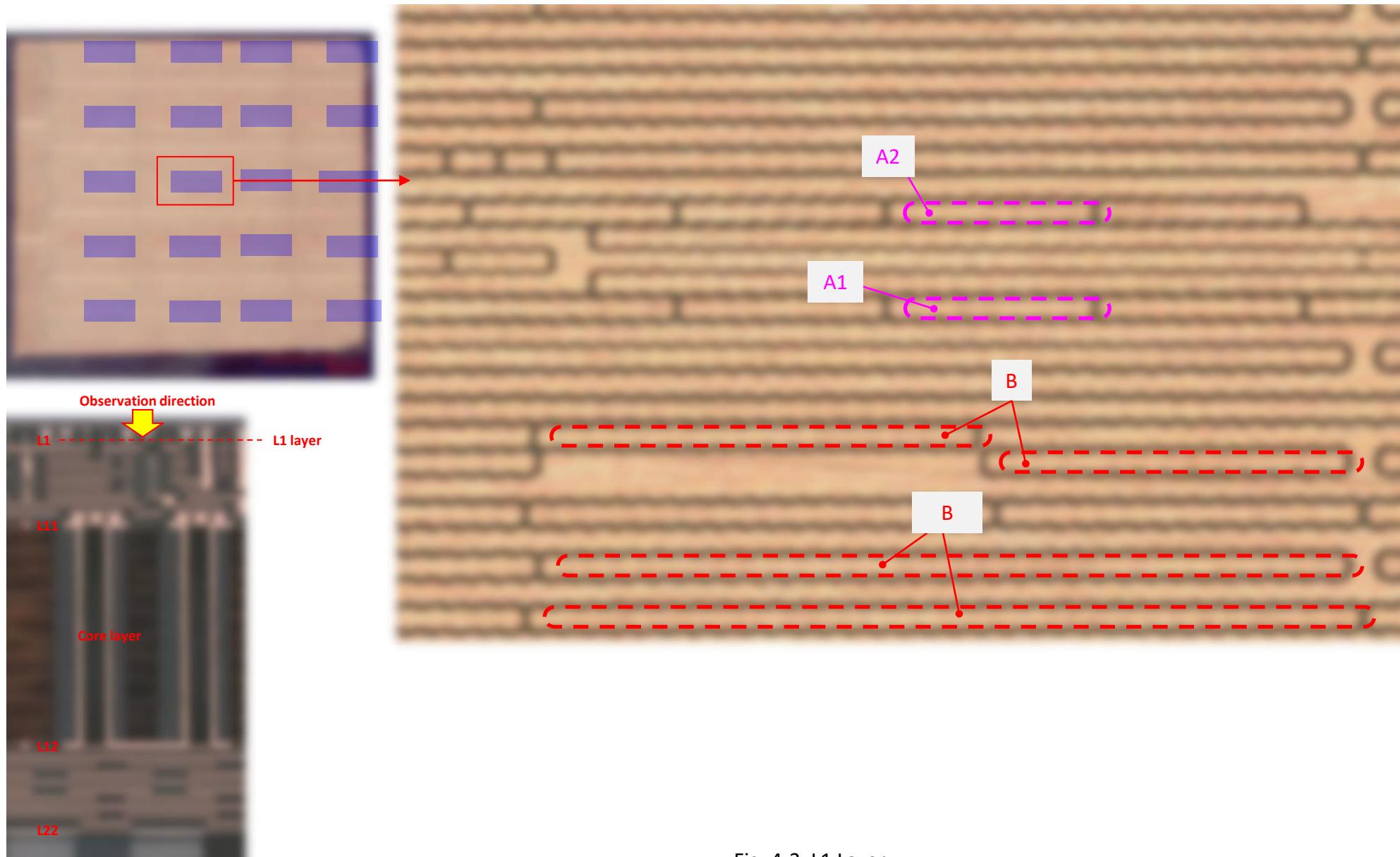


Fig. 4-3 L1 Layer

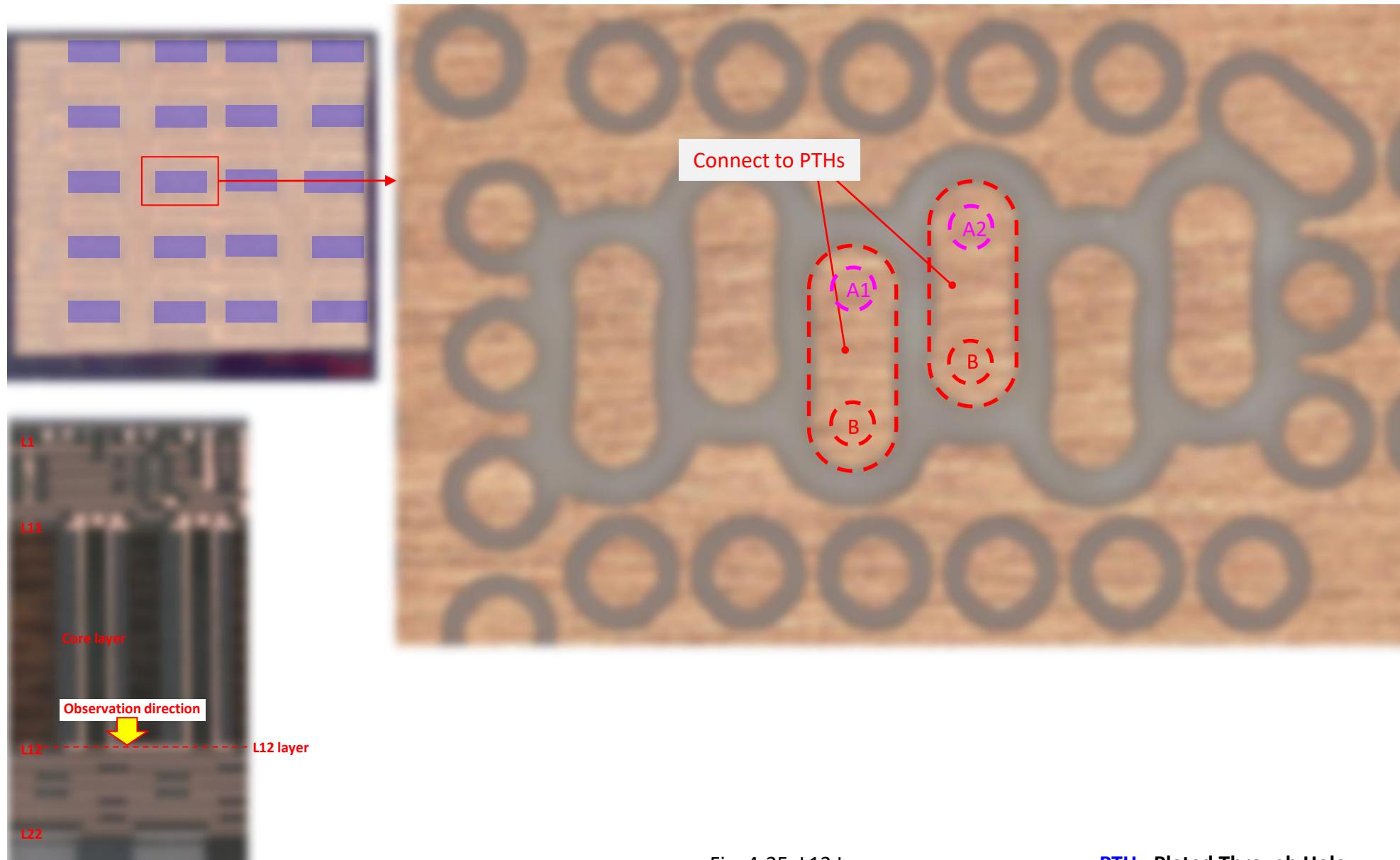


Fig. 4-25 L12 Layer

PTH : Plated Through Hole

## 5. Schematic diagram

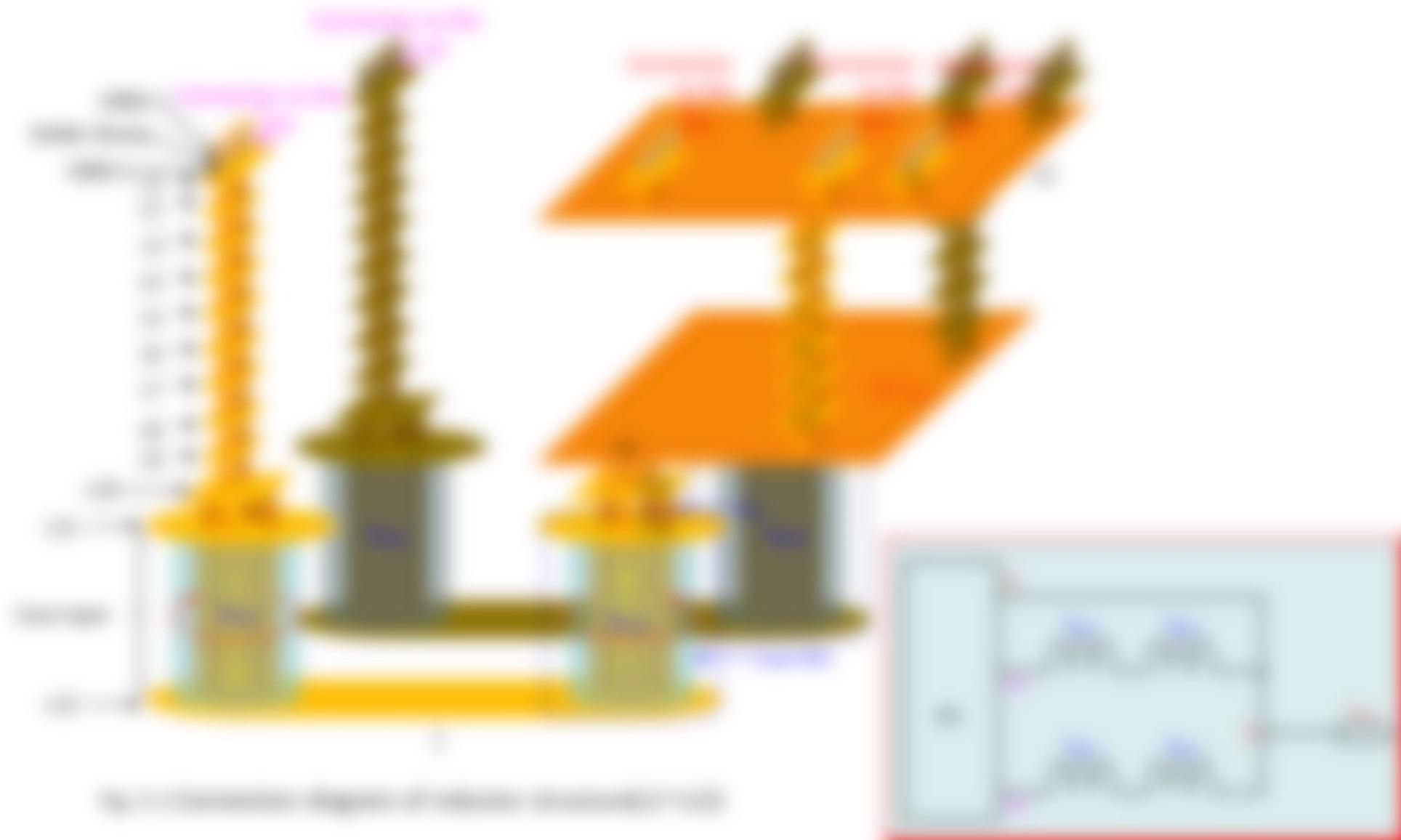


Fig. 5-2 Equivalent circuit of interconnect and inductors

## 6. Cross-section

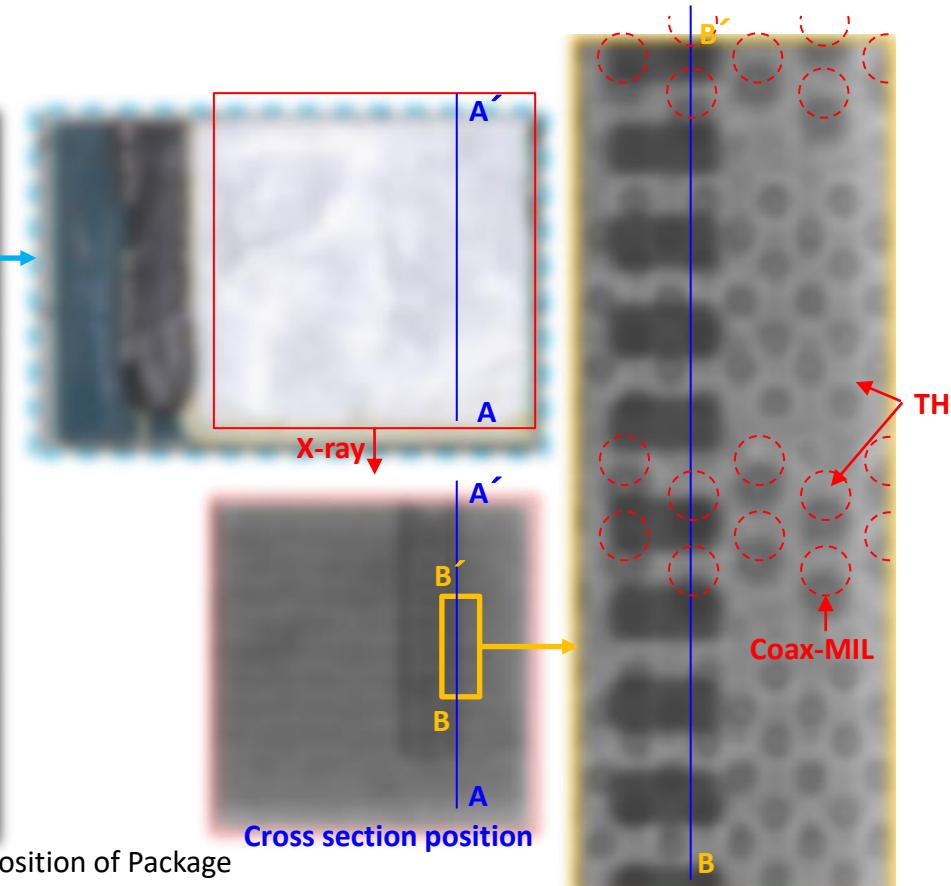
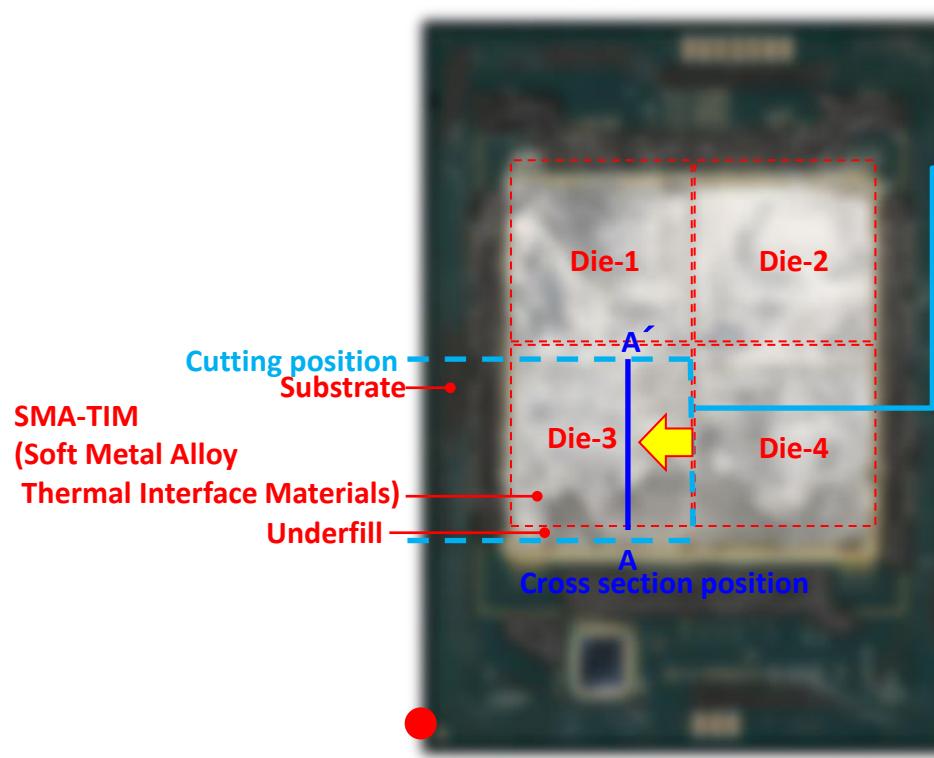


Fig. 6-1 Cross-section position of Package

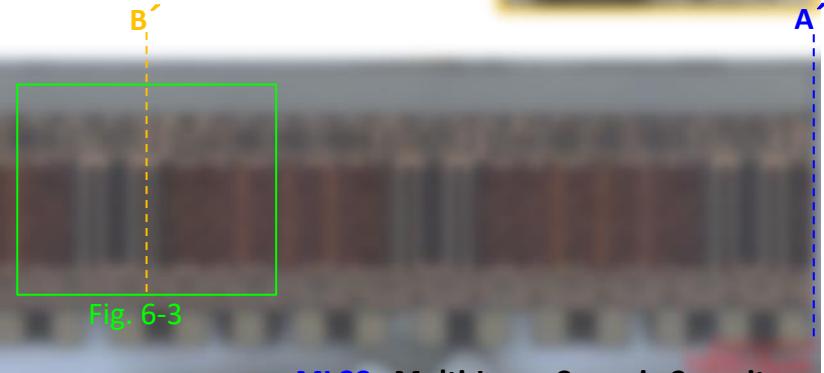
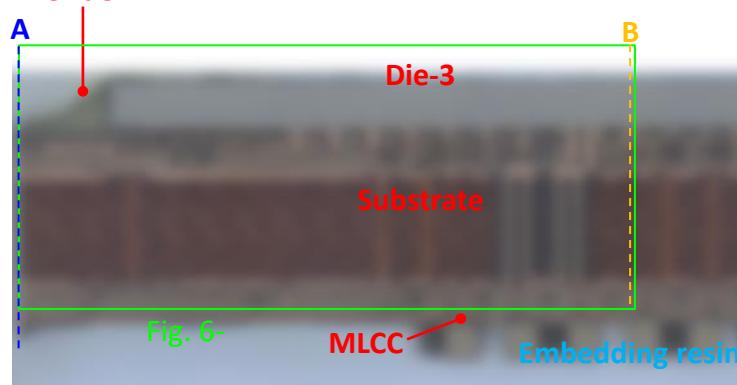


Fig. 6-2 Image of Cross-section

**MLCC** : Multi-Layer Ceramic Capacitor

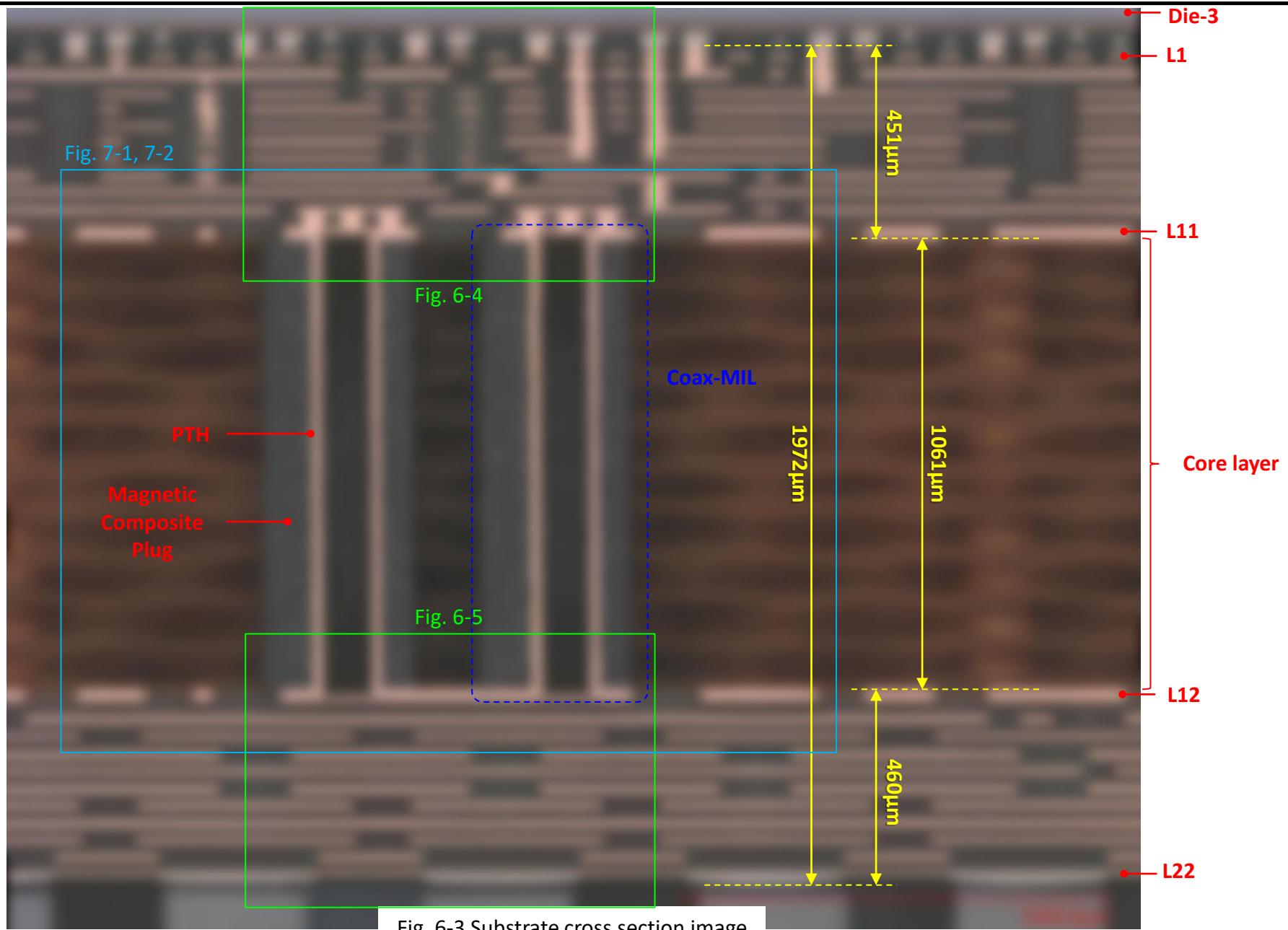




Fig. 6-9 Micro-bump cross-section image

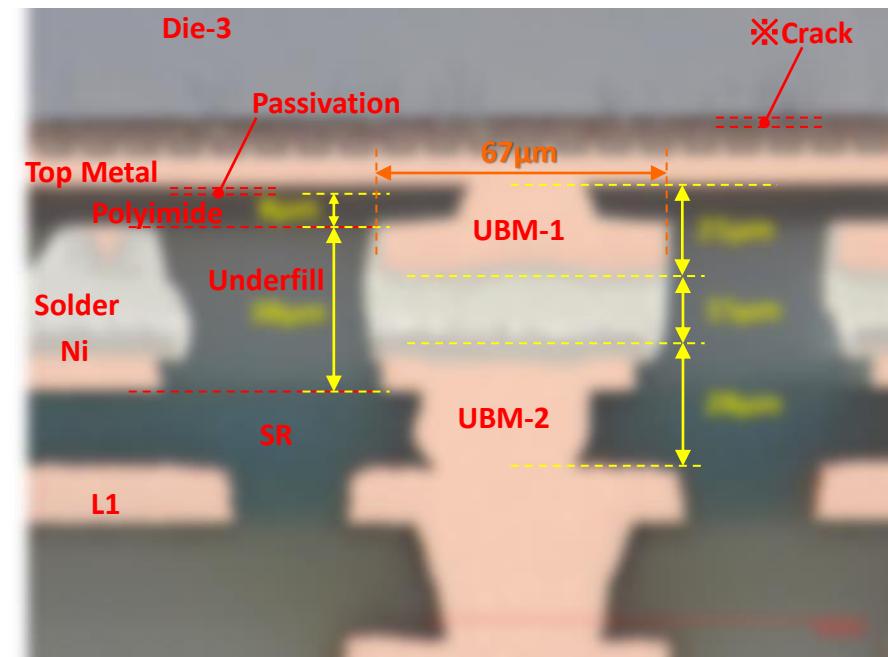


Fig. 6-10 Micro-bump cross-section image

## 7. Coax-MIL inductor material analysis (EDX)

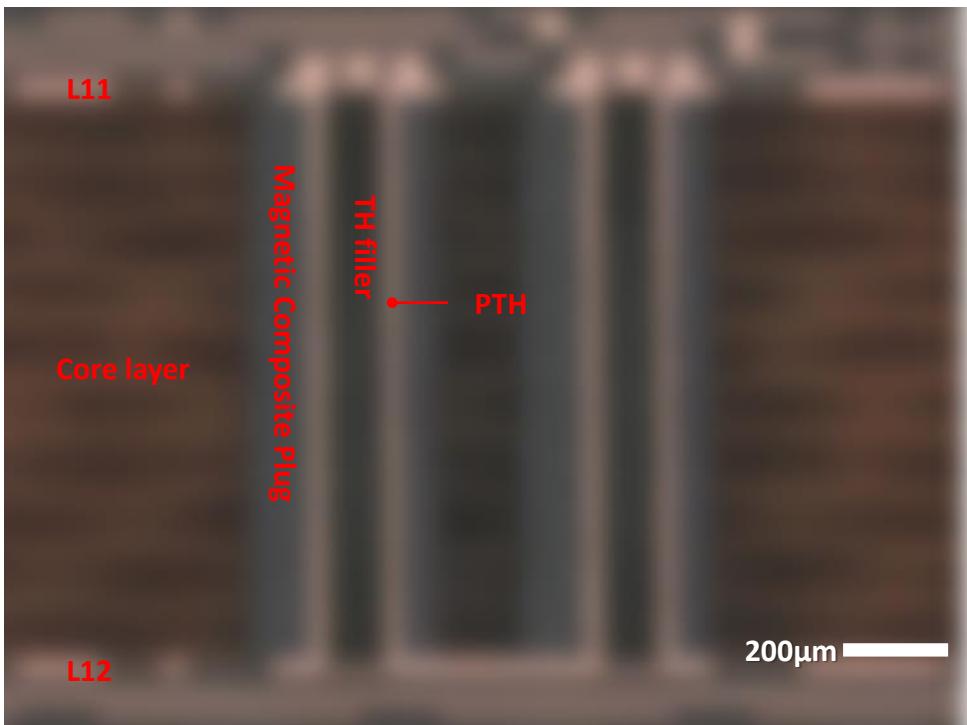


Fig. 7-1 Coax MIL cross-section image

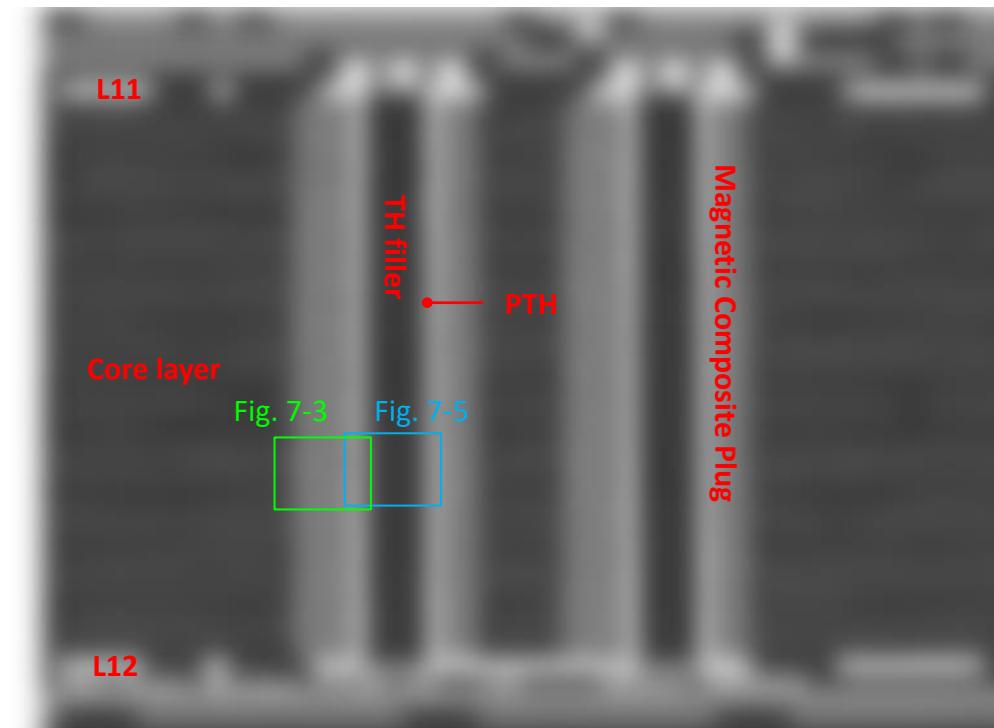


Fig. 7-2 Coax MIL SEM image

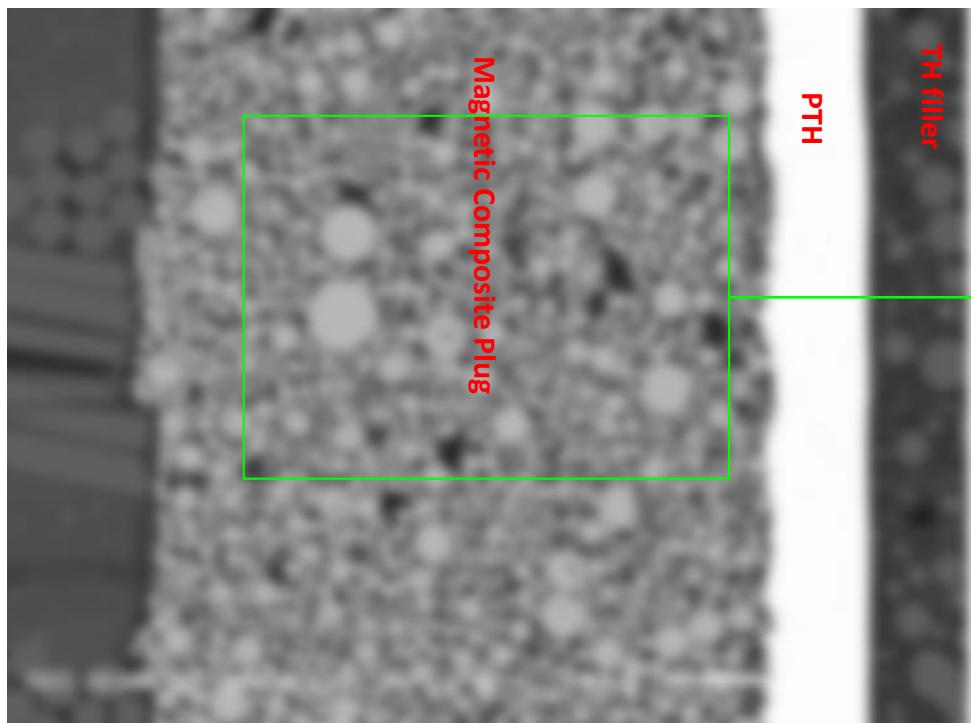


Fig. 7-3 Coax MIL SEM image

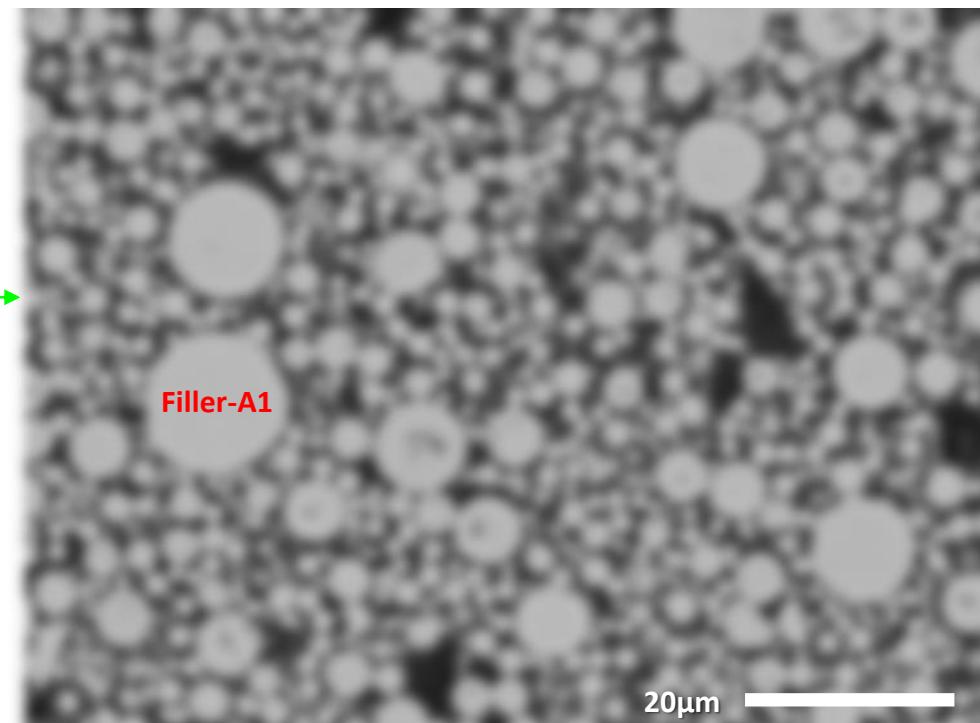


Fig. 7-4 Coax MIL SEM image

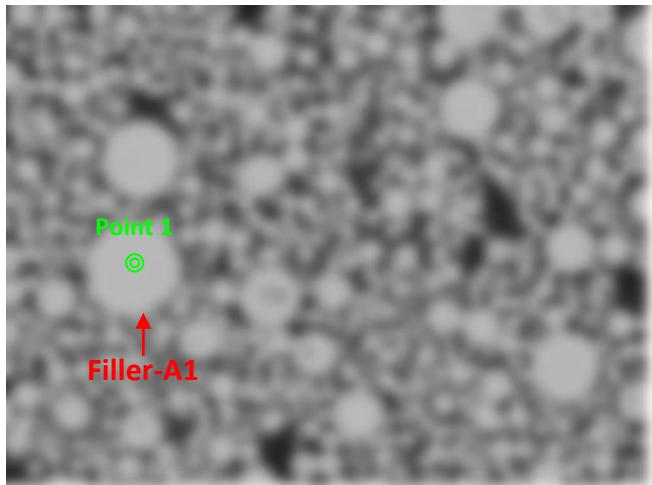
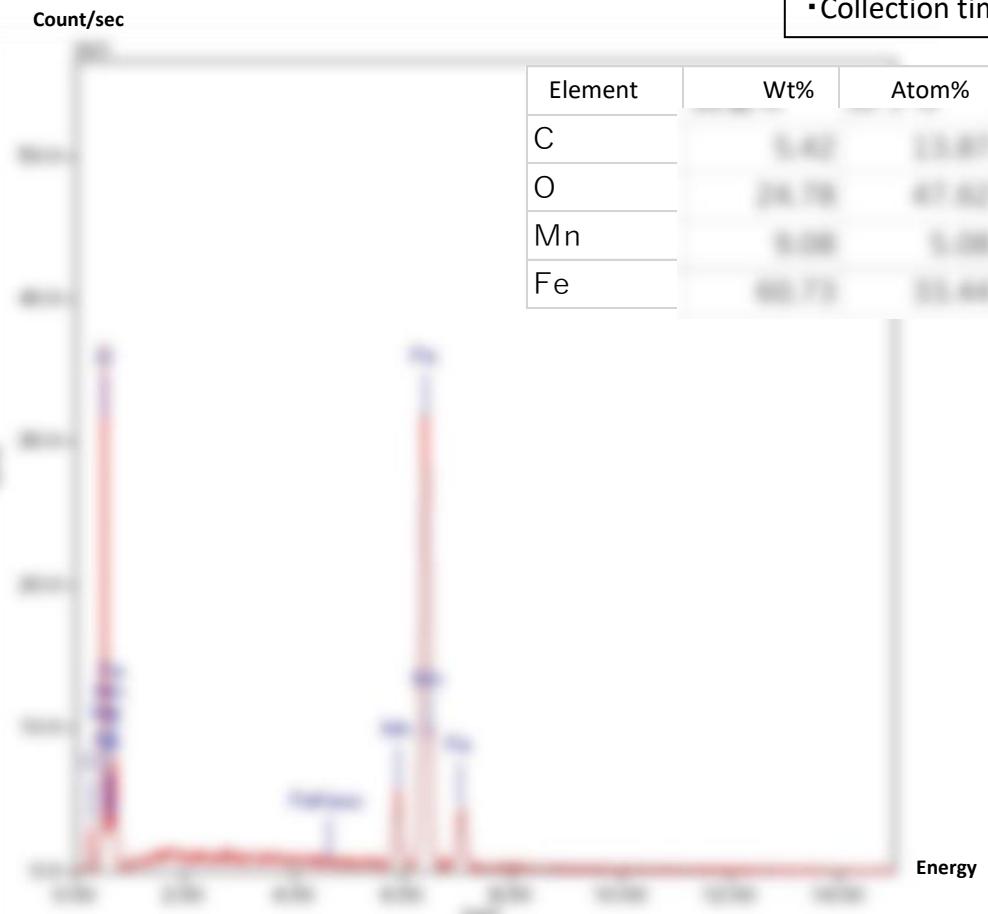
Point 1

Fig. 7-7 Coax-MIL Filler Analysis point1

Analysis conditions

- Acceleration voltage: 20kV
- Collection time: 10min



## [EDX Analysis result ]

**main elements**

(O, Mn, Fe, Si, Al, Ti, Cr, Ni, Cu, Zn, Sn, Pb, As, Sb, Bi, Ag, Au, Pt, Pd, Hg, Cd, In, Tl, Ge, Te, S, C)

**Other detected elements :****C (Carbon coat for conduction)**

Fig. 7-8 EDX spectrum result Point 1

**Appendix (1): Comparison with ACIs and Coax MIL [Xeon Gold 6430, Xeon Silver 4310, Alder lake]**

Xeon Gold 6430

( 22 layer [ 1972um(t) ] )

[ 4th Gen intel Xeon ]

Inductor uses core layer

Xeon Silver 4310

( 22 layer [ 1660um(t) ] )

[ 3rd Gen intel Xeon ]

Alder lake

( 10 layer [ 1150um(t) ] )

[ 12th Gen Core i7 ]

Inductor layers used: L6-10

Coax MIL

Air Core Inductor

L11 – Core layer - L12 [ 1115um(t) ]

L11 – Core layer – L12 ~ L17 [ 1000um(t) ]

L6 ~ L10 [ 203um(t) ]

## Appendix (2): References

- ① Integrated Voltage Regulator Efficiency Improvement using Novel Magnetic Composite Core Inductors  
" 2002-2003 Power Electronic Components and Technology Conference (PEC)"

### 2. ( Related patents )

- "Magnetic collector device and method"
- "Electrode and/or resistor with dual-sided and unidirectional current flow"
- "Current sense resistors for monitoring voltages within a package"
- "Resistor with two resistive materials in series"