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# 1. Overview

## 1-1. Device Summary

**Table 1 Device Summary**

Category	Battery Management IC
Product Name	BQ79616-Q1
Manufacturer	Texas Instruments
Package Type	TQFP-66 (with Heat Sink)
Package Marking	16C14796 BQ79616 04
Die Marking	00 2020 BQ79616B1
Die Size	4.88mm x 4.82mm = 23.49mm <sup>2</sup>
Process Type	BiCMOS
Layers	Poly (Silicon) 6/10/6/1/6
Minimum Gate Length	0.2 μm (半導體製程技術)

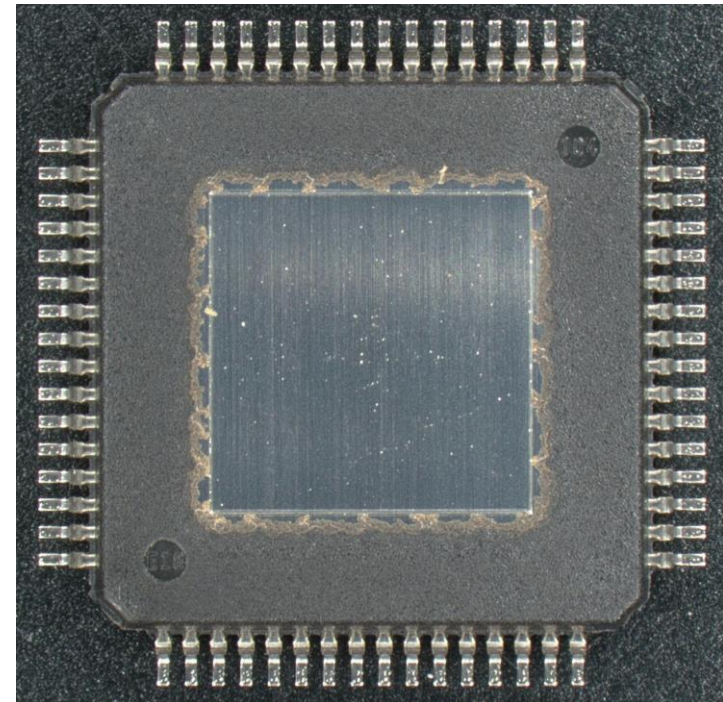
## 1-2. Package

● 1Pin



●

**Fig. 1-2-1 Package (Top View)**

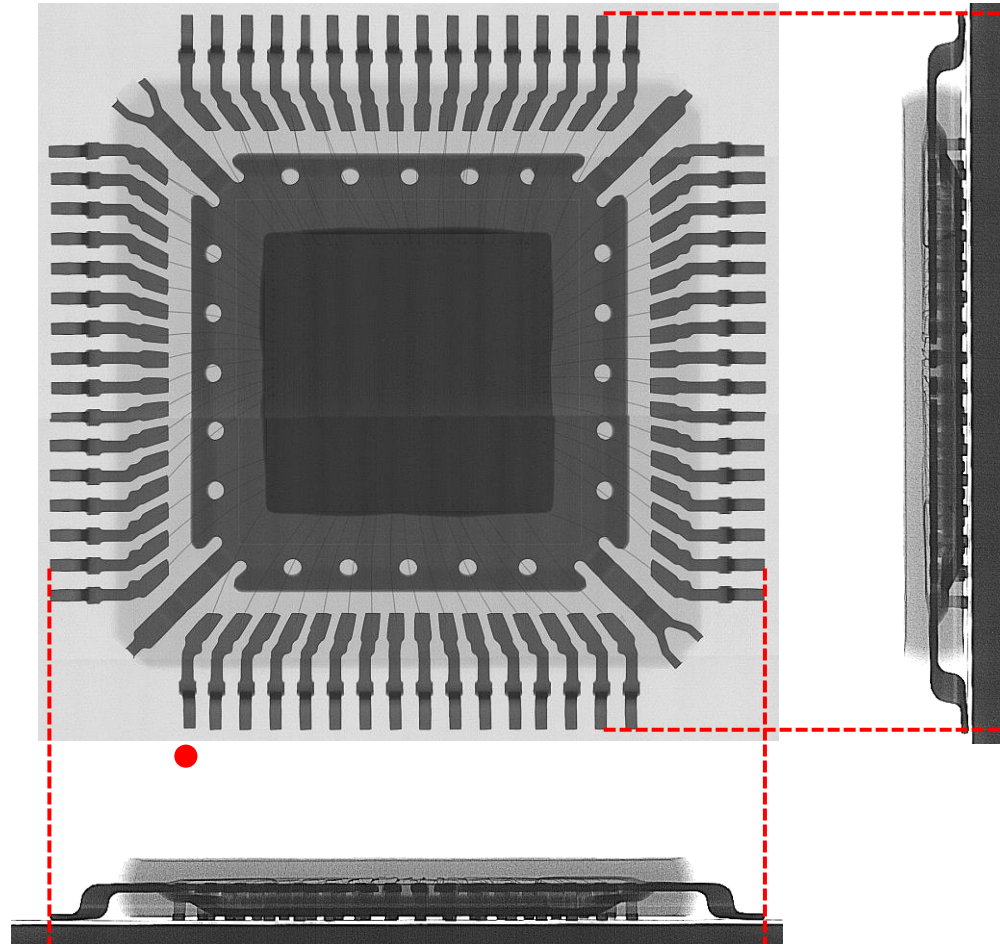


●

**Fig. 1-2-2 Package (Bottom View)**

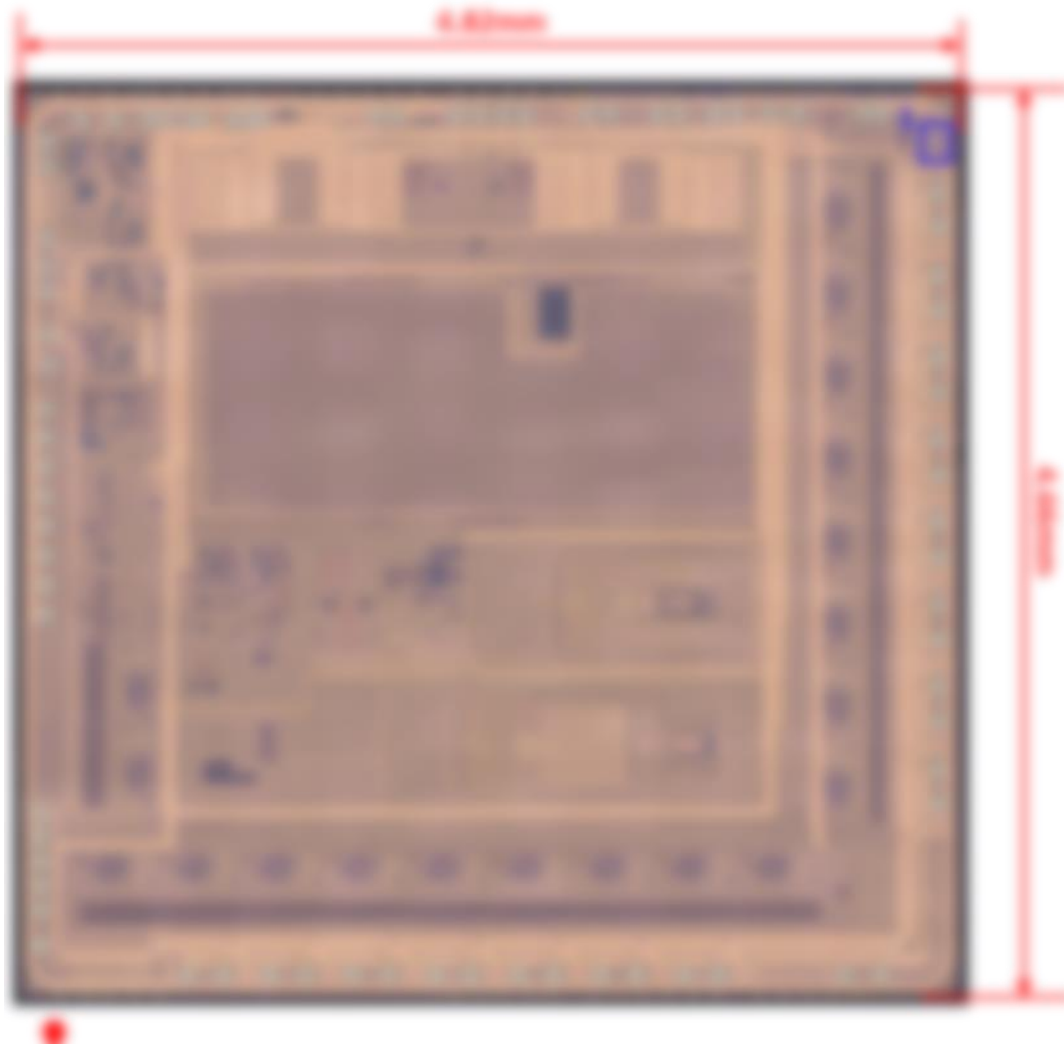
**1-3. Package X-Ray**

● 1Pin



**Fig. 1-3 Package X-Ray**

## 1-4. Die Overview

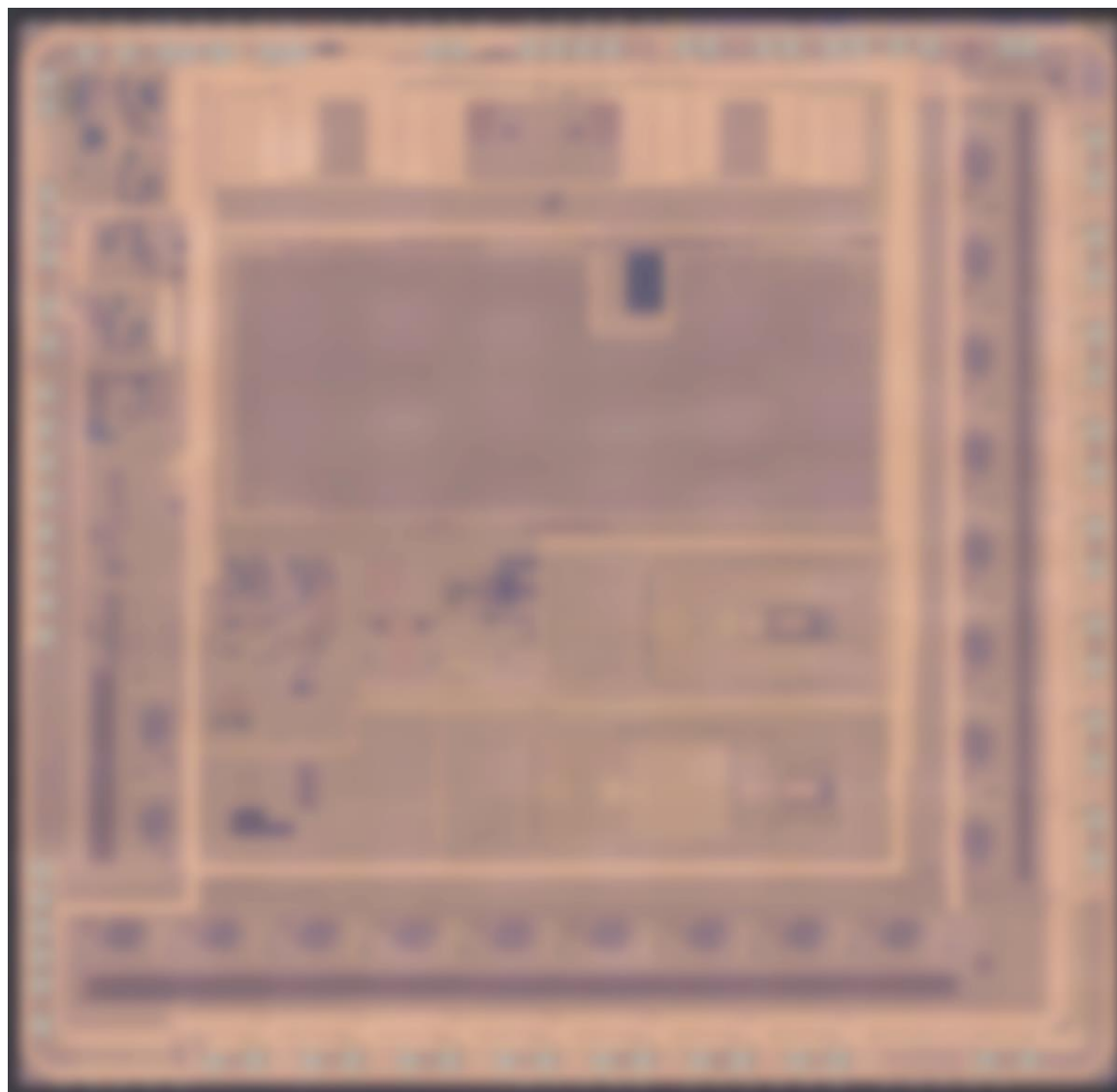


**Fig. 1-4-1 Die Size (5th Metal Layer)**



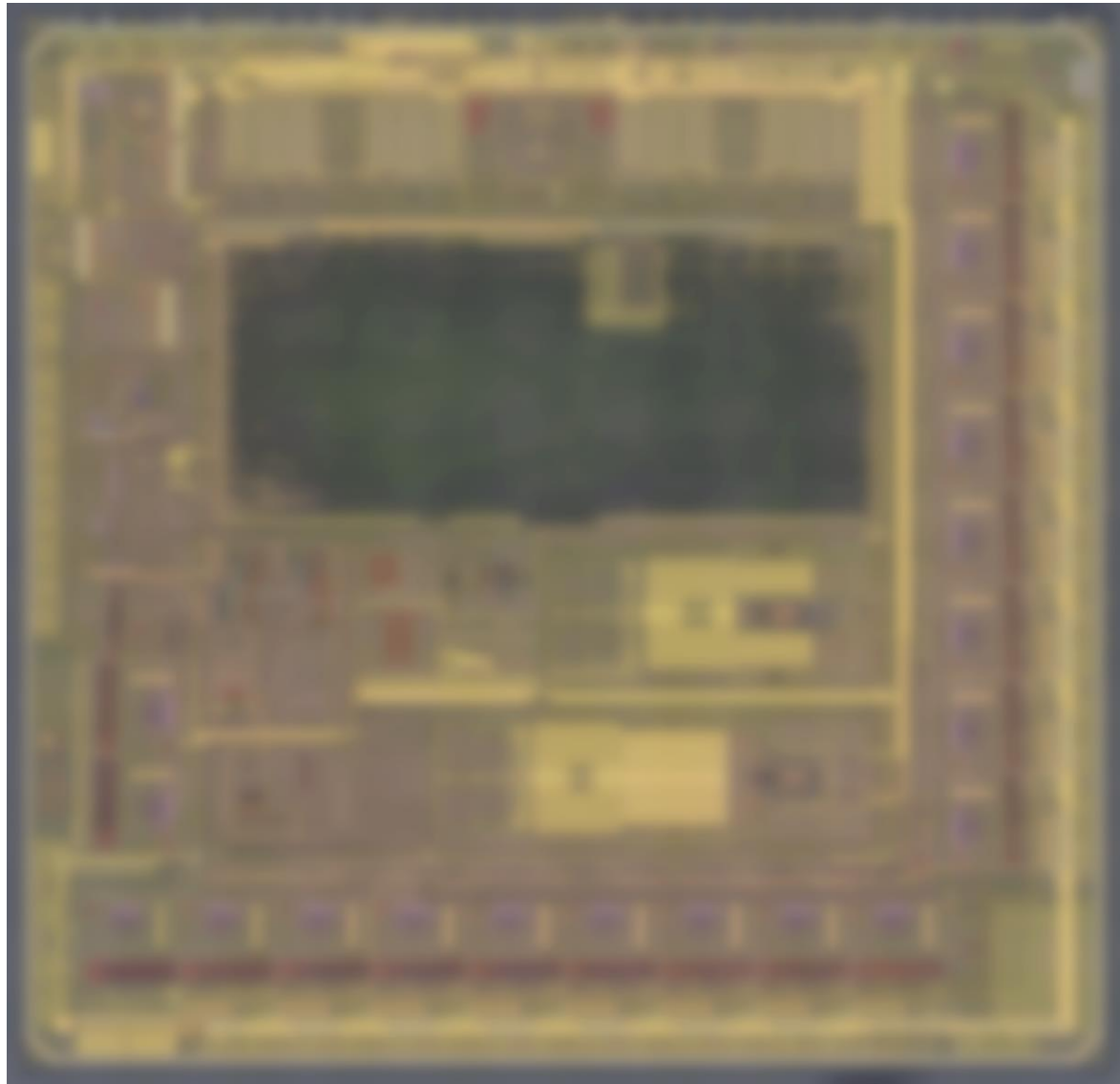
※Fig. 1-4-1よりCW方向に90度回転

**Fig. 1-4-2 Die Marking**

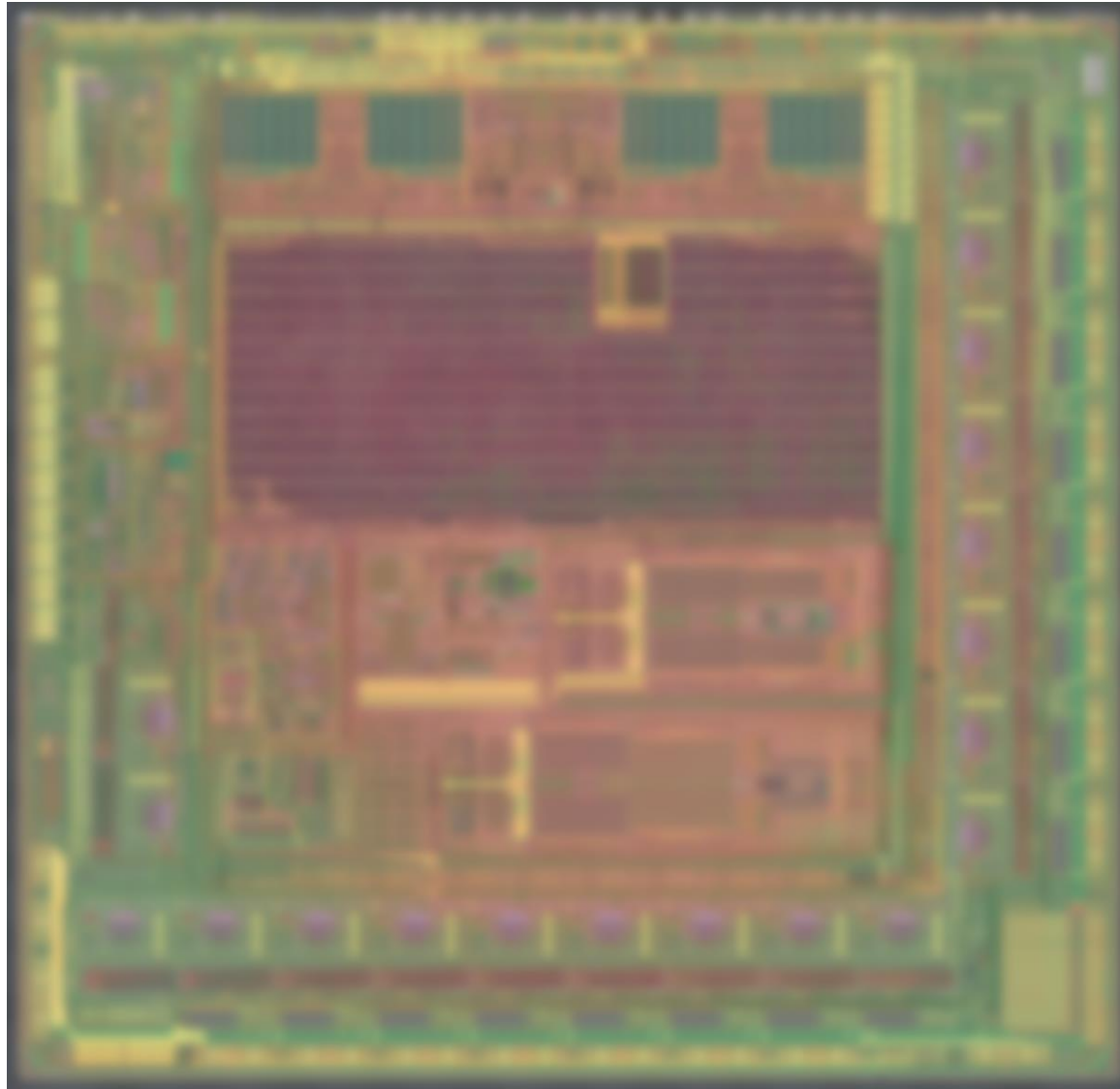


**Fig. 1-4-3 Die Overview (5th Metal Layer)**

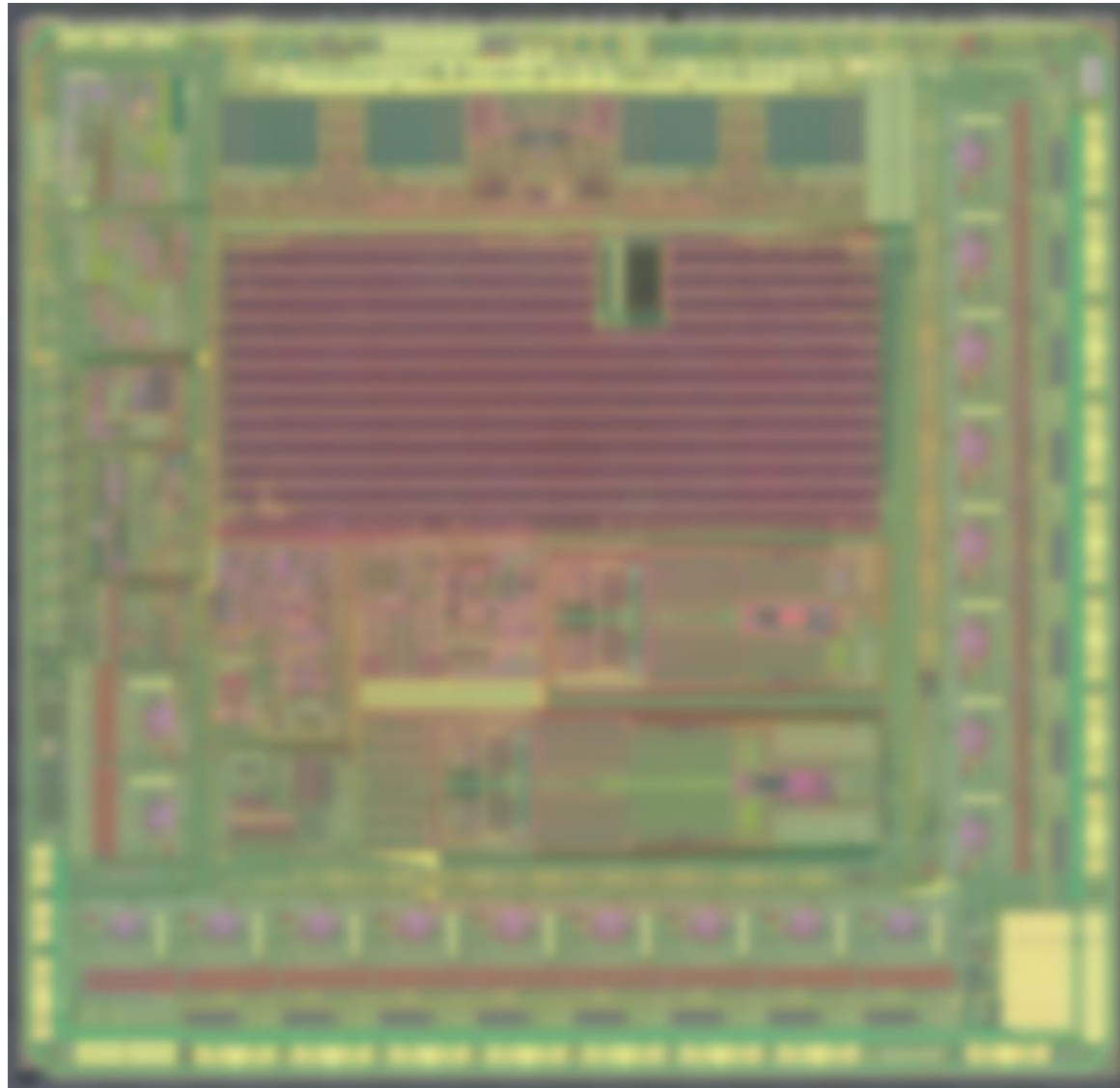




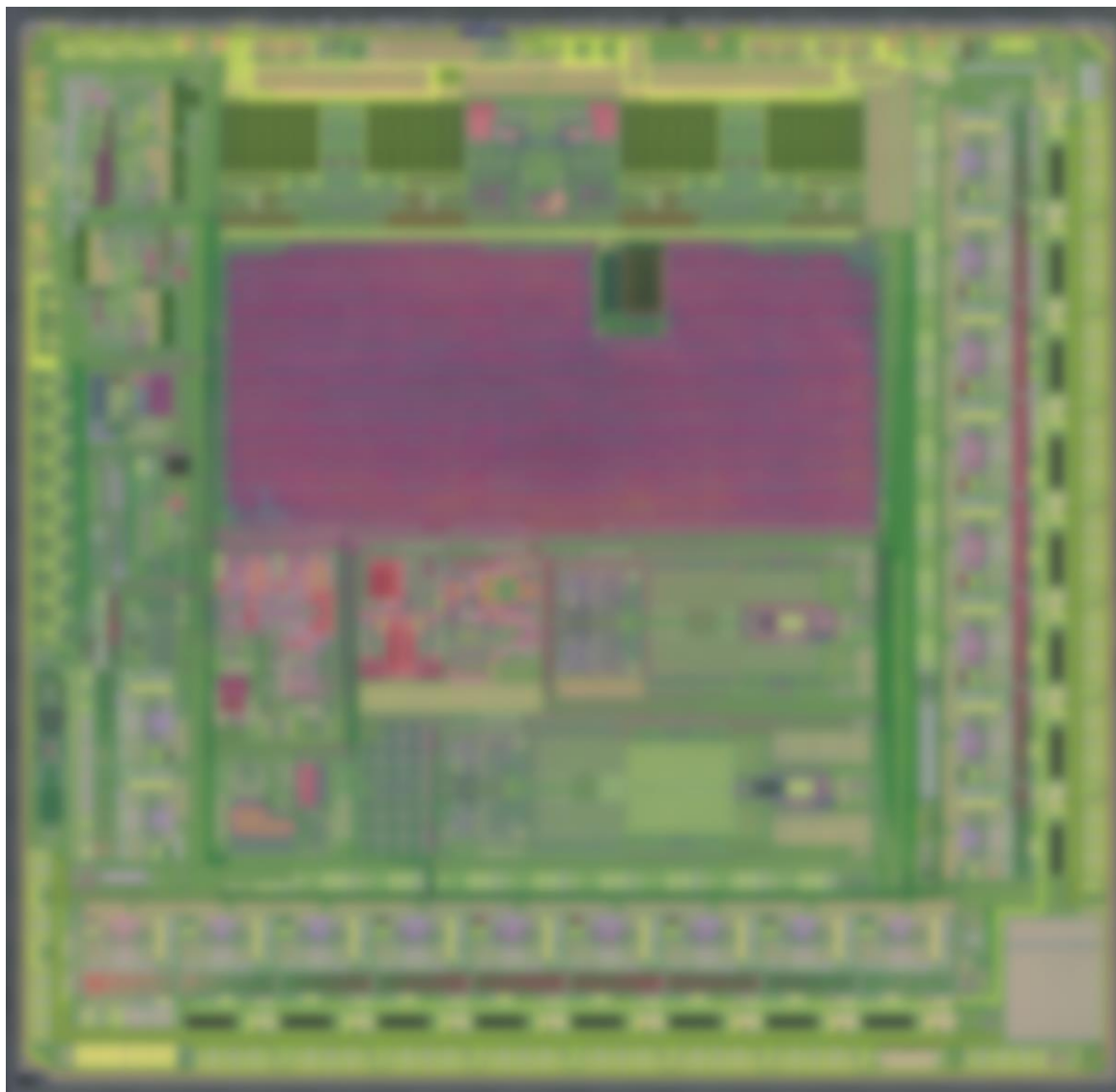
**Fig. 1-4-4 Die Overview (4th Metal Layer)**



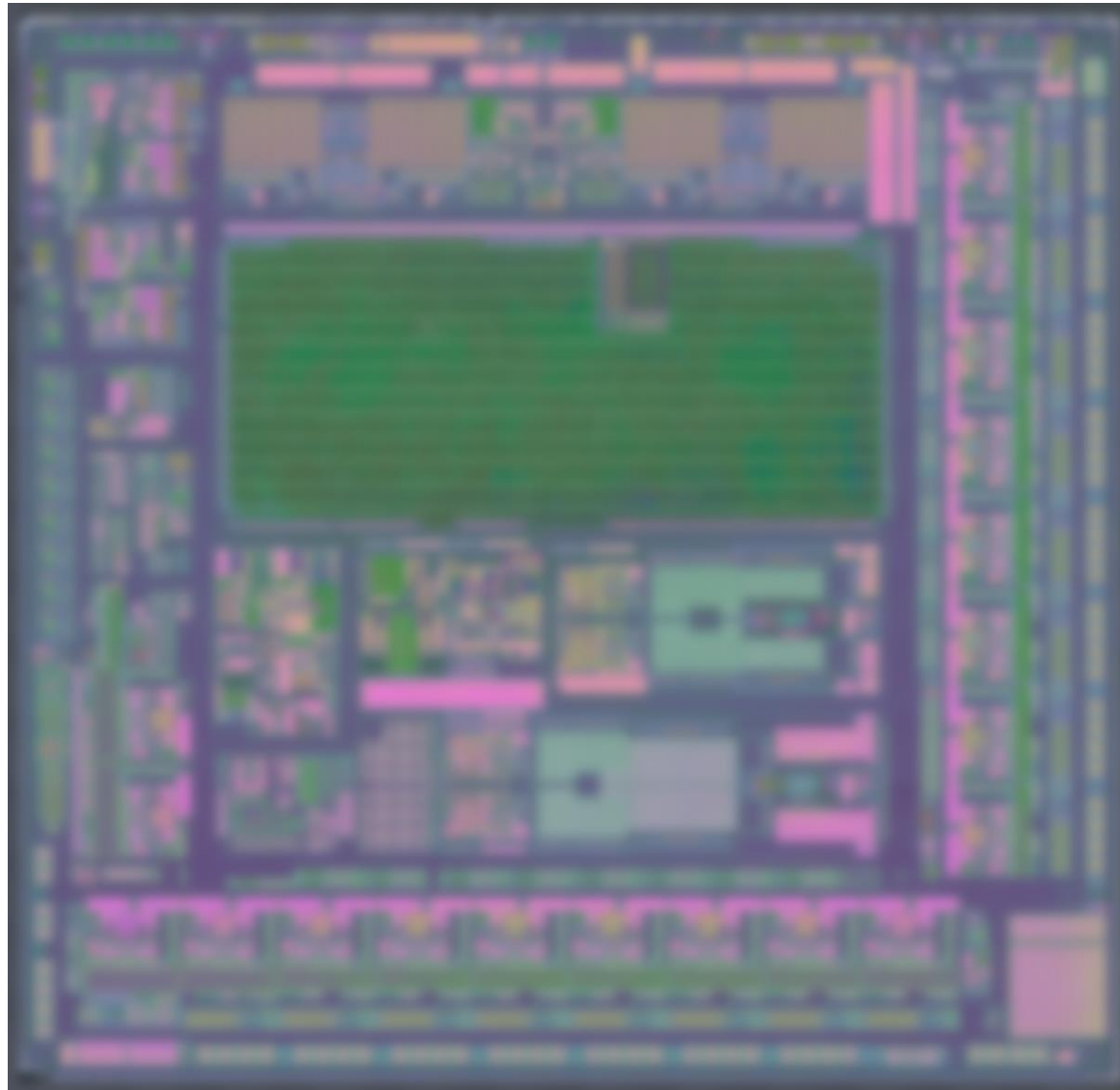
**Fig. 1-4-5 Die Overview (3rd Metal Layer)**



**Fig. 1-4-6 Die Overview (2nd Metal Layer)**



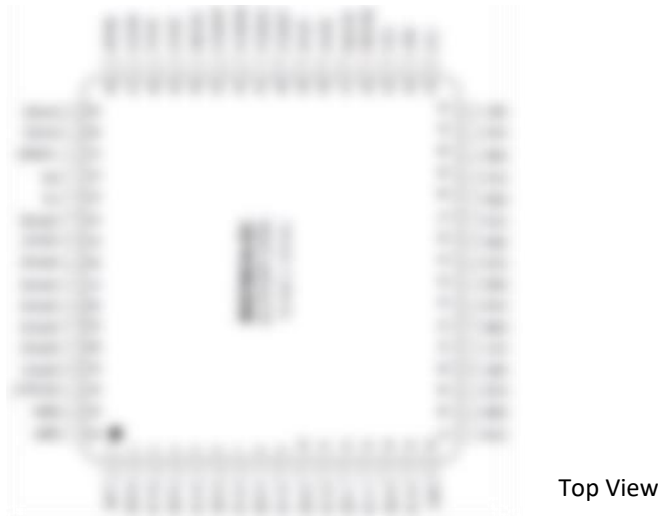
**Fig. 1-4-7 Die Overview (1st Metal Layer)**



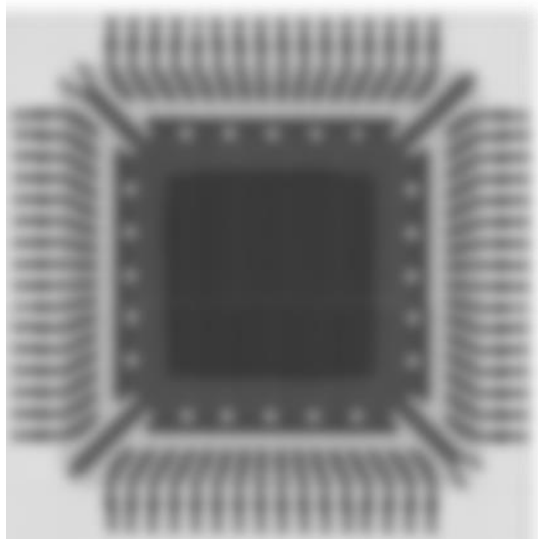
**Fig. 1-4-8 Die Overview (Poly-Si Layer)**

## 1-5. Pin Assignment

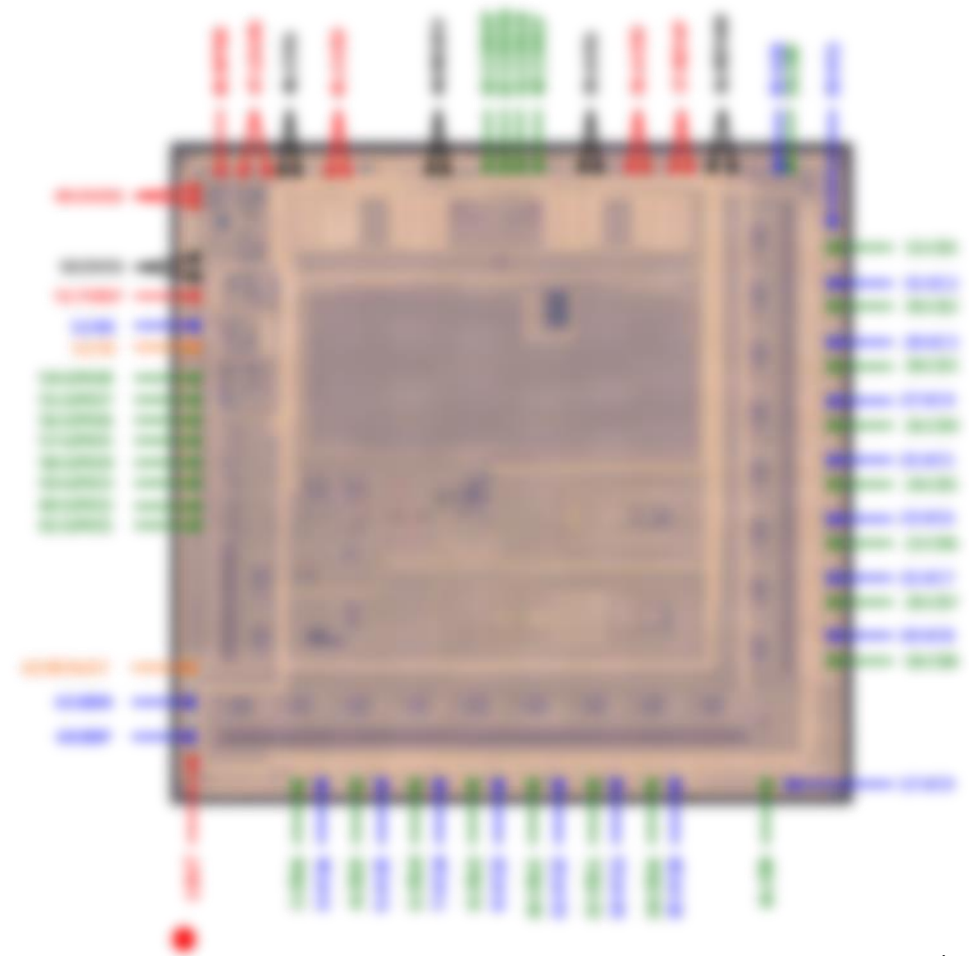
● 1Pin



**Fig. 1-5-1 Pin Assignment (Datasheet)**



**Fig. 1-5-2 Pin Assignment (X-Ray)**



**Fig. 1-5-3 Pin Assignment (Die Overview)**

## 2. Elements

### 2-1. MOS Transistor

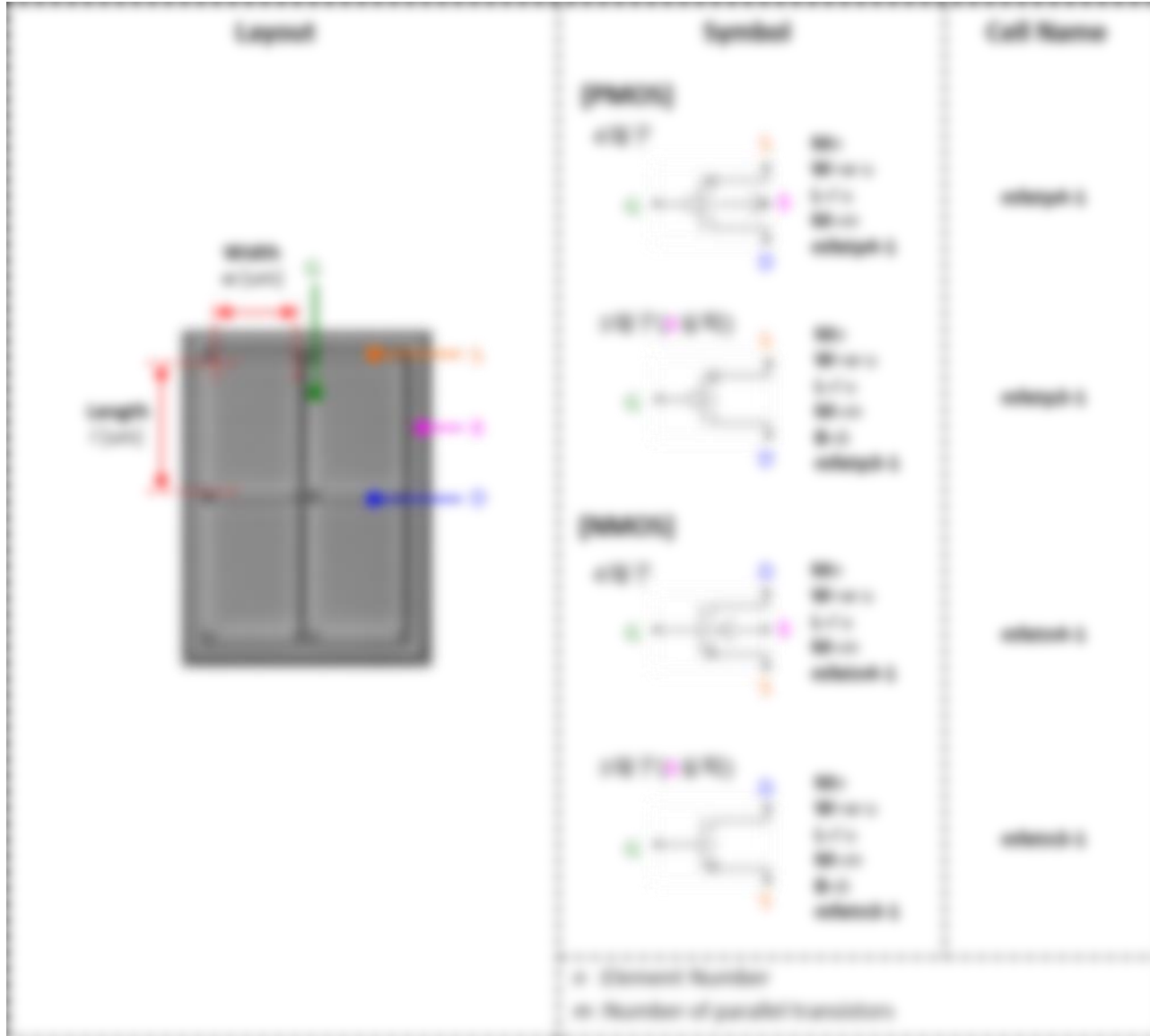
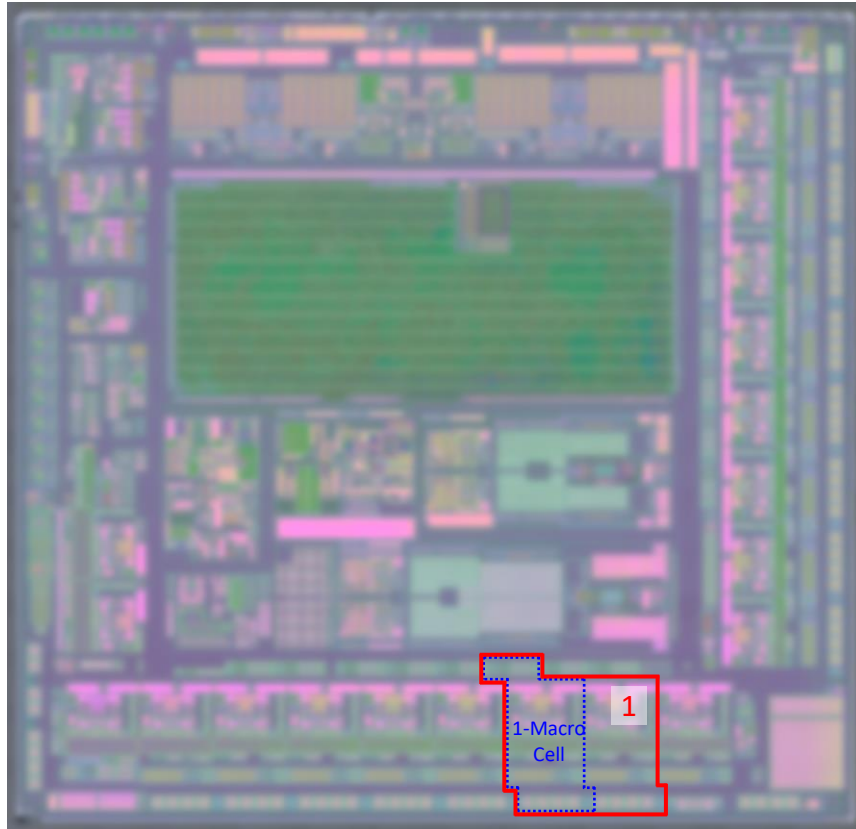


Fig. 2-1-1 MOS Transistor

### 3. Analysis Area



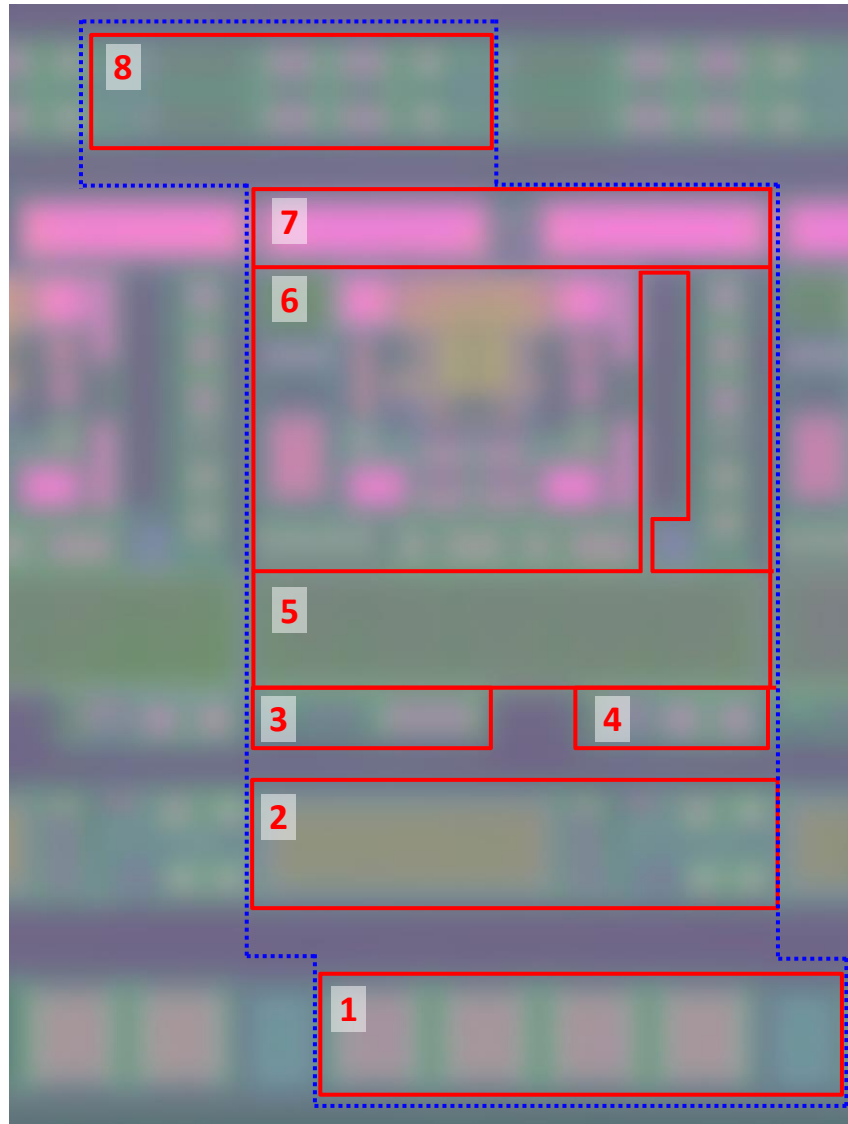
Poly-Si Layer

**Fig. 3-1 Analysis Area**


**Table 3-1 Function**

No.	Function	Fig.
1	Cell Monitor & Cell Balancing	5



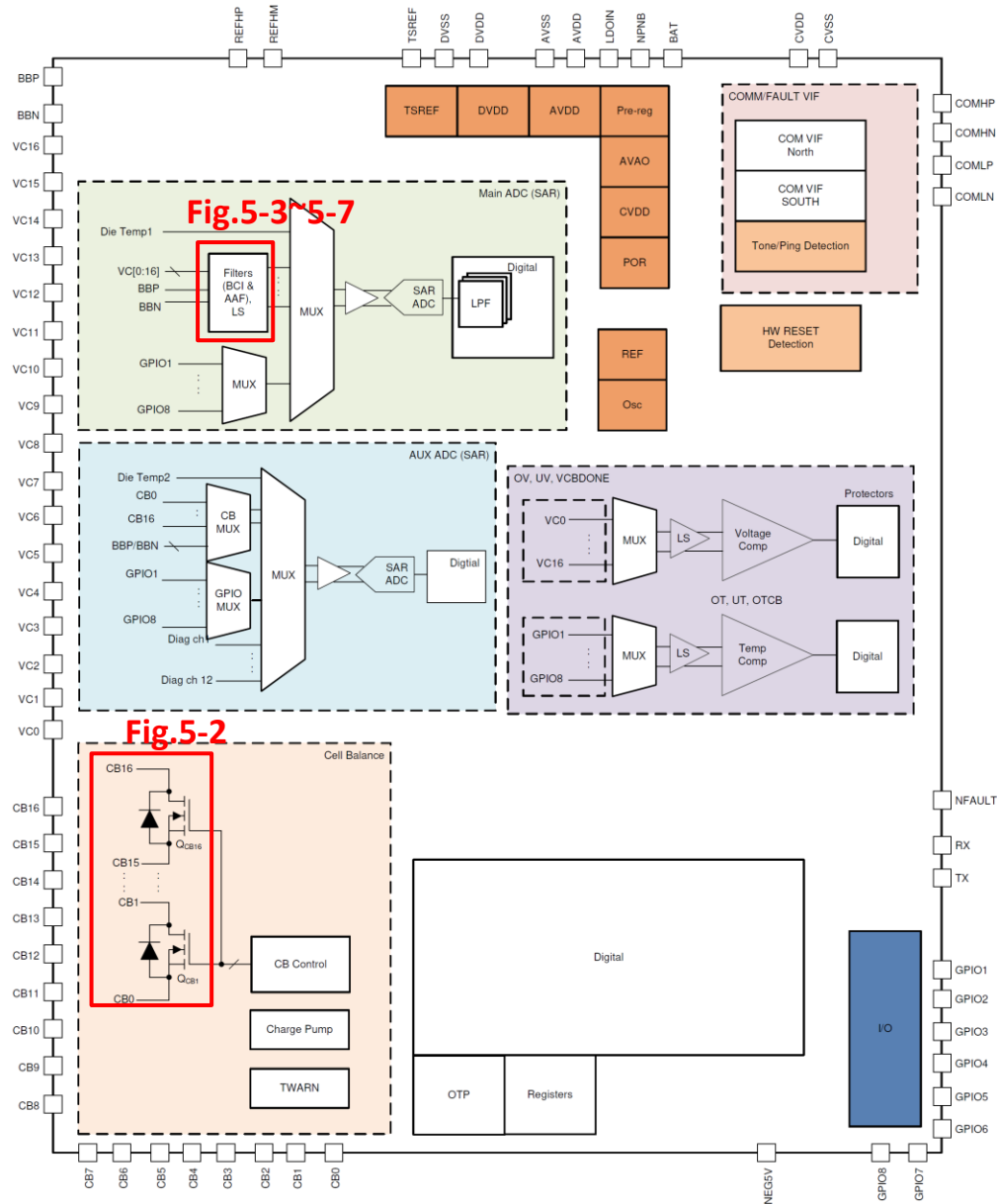
**Table 3-2 Function**

No.	Function	Fig.
1	ESD Protection Circuit	5-1
2	Cell Balance Circuit	5-2
3	VC Input Switch	5-3
4	Open Wire Check	5-4
5	Low Pass Filter, Unused Resistor	5-5, 5-9
6	Level Shift Buffer	5-6
7	AAF	5-7
8	CB Input Switch	5-8

 1-Macro Cell Area

Poly-Si Layer

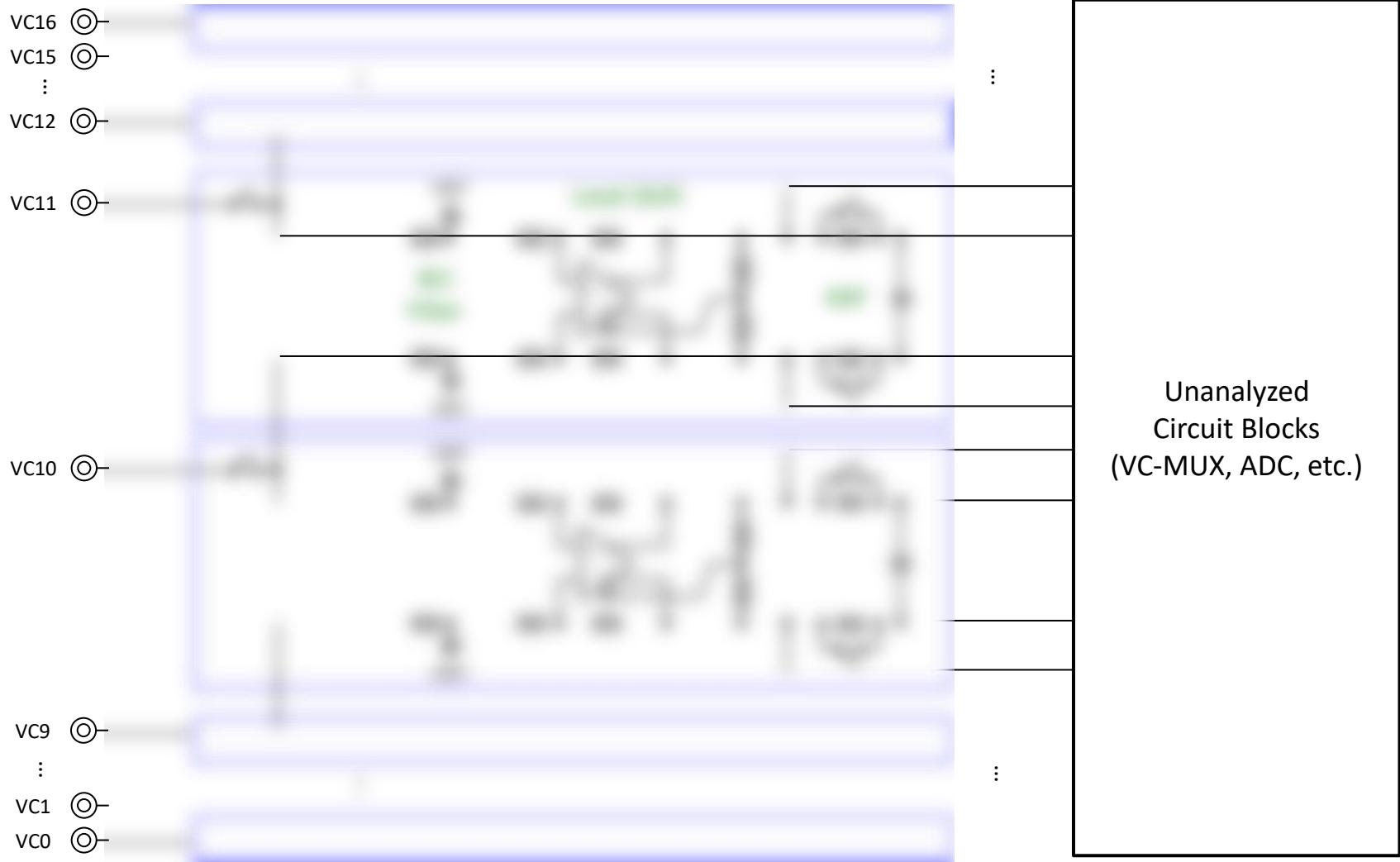
**Fig. 3-2 Cell Monitor & Cell Balancing Block (1-Macro Cell)**




**Fig. 3-3 Functional Block Diagram (vs Datasheet)**

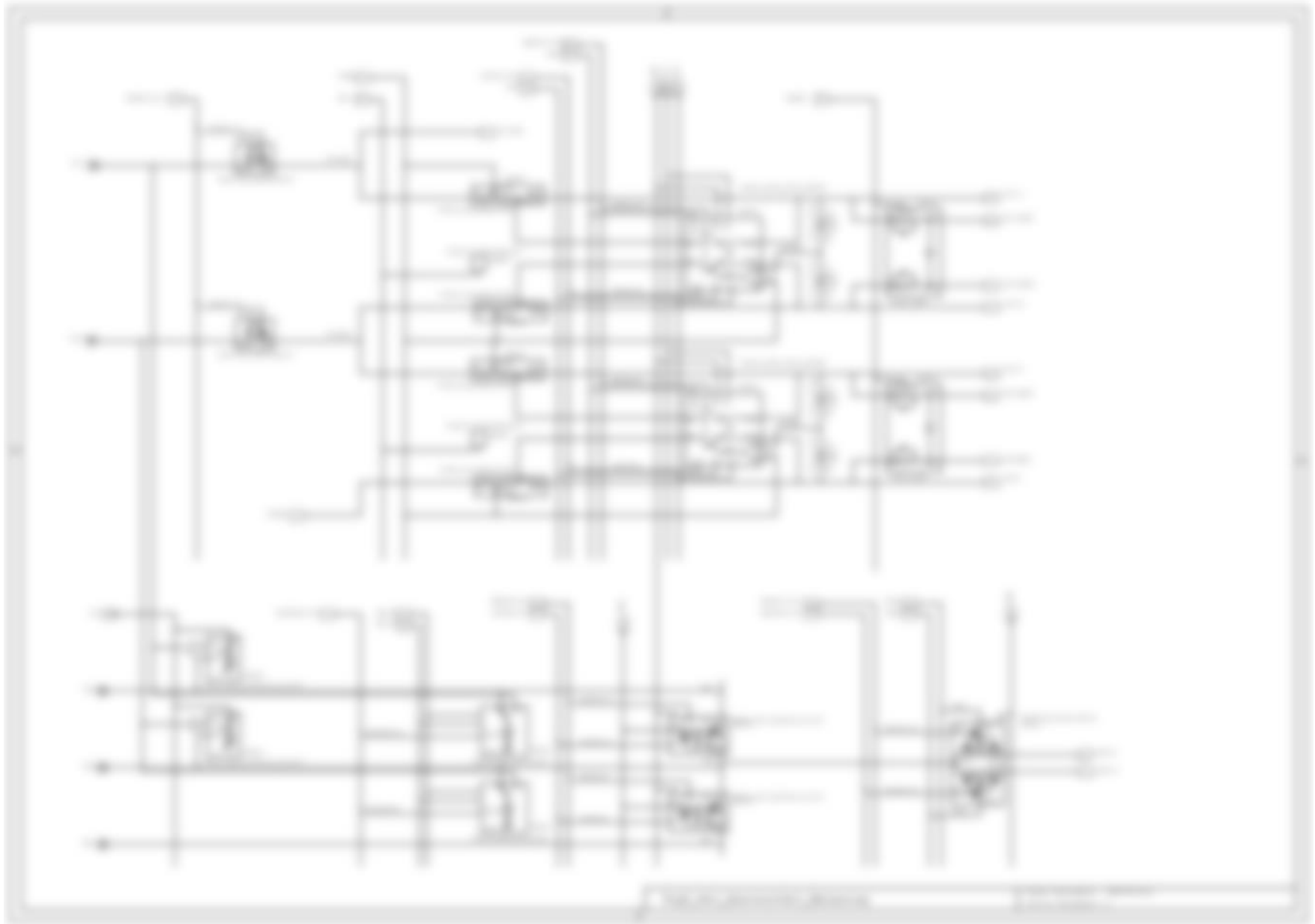
### 4. Circuits

Fig.5-3 ~ 5-7



 1-Macro Cell Block

**Fig. 4-1 Simple Block Diagram of Cell Monitor**



■ Return to Previous Circuit [Fig. 5]

