

Product Analysis Report

No.22G-0037-2 Onsemi NTH4L022N120M3S Process and Electrical Characteristics Analysis
Product : SiC MOSFET
Part No. : NTH4L022N120M3S
Manufacturer : ON Semiconductor Corporation
Die size : SiC MOSFET
Process : SiC wafer, Planer Gate, Top Metal Source, Double metal process

This report is a process flow analysis report based on the structure analysis results of Report 22G-0018-1, and it includes the following contents,

- I. Estimating process manufacturing sequence of SiC MOSFET and photo/masking process steps
- II. Considerations on the main process features.
- III. Doping concentration profile analysis of the extracted N-epi layer.
- IV. Correlation between device structure and electrical characteristics.

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1. Onsemi's SiC MOSFET NTH4L022N120M3S: Summary of analysis results

Based on the structural analysis results of onsemi's 1200V 40A Non-Cooled "Wide-Channel" SiC MOSFET device (NTH4L022N120M3S),

- Determine the manufacturing process flow
- Estimate the number of photo-/masking process steps
- Investigate the important characteristics of the transistor.

The 1200V "Wide-Channel" product is the first member of the onsemi 400V SiC family released in 2022. 400V SiC transistors are also used in the company's 600V power modules.

Main results

1. The SiC MOSFET has a maximum operating voltage of $V_{DS} = 1200V$ and an on-resistance per unit area of $R_{DS(on)} = 20m\Omega/cm^2$ (transistor active area). The low $R_{DS(on)}$ value is comparable to 8th generation SiC processes from other manufacturers. Fig. 1 summarizes the comparison of SiC MOSFETs from each manufacturer.
2. Compared to the company's previous generation SiC MOSFET family, the transistor cells are reduced 50% (the 400V process reduces the pitch by 50%). In addition, a two-layer metal process is used to efficiently utilize the chip area. This metal configuration allows a large gate pad to be formed over the active area of the transistor.
3. Drain-gate feedback capacitance (gate-drain), which can commonly cause false turn-on problems, is greatly reduced by using a "thick oxide" stack on the W_{DG} area. The self-aligned formation of this "thick oxide" stack has been analyzed and demonstrated.
4. The SiC MOSFET is fabricated with an 8-layer SiC epitaxial layer with a thickness of 8.2 μm and a doping concentration of about $1 \times 10^{18} cm^{-3}$ to achieve a drain breakdown voltage $V_{DS} = 1200V$.
5. It is estimated that 17 photo/masks are used in the first half of the process up to the backside metal process.
6. MOSFET channel length and field (loop) back offset are formed self-aligned.
It is assumed that the process consists of a hard mask and the channel length (pitch) back is determined by the tilted/laser spacer method.
7. Source region (drain W_{DG}) is formed using a separate mask than metal (SiC) contact openings.
8. The magnitude of the drain leakage current @ 1200V is comparable to other SiC transistors, but it is 2-3 orders of magnitude lower than the off-current of Si MOSFET. The temperature dependence shows an activation energy of 0.7 eV.

1-1. Comparison of characteristics between onsemi M3S and other companies' SiC MOSFETs.

Maker	Part no.	Process Gen	Product ion	Die Size mmxmm	mm2	Vdss [V]	RON [mΩ]	Intrinsic RONxA [mΩ·mm ²]
ROHM	SCT2080KE	3rd	2012	4.27x2.05	8.75	1200	40	350
ROHM	SCT3080KL	3rd	2016	3.25x2.45	7.96	1200	40	318
ROHM	SCT4062KR	4th	2012	2.85x2.25	6.41	1200	40	257
WOLFSPEED (CREE)	C3M0075120K	3rd	2017	3.44x2.75	9.47	1200	75	340
INFINEON	AIMW120R060M1H	3rd	2012	3.77x2.27	8.56	1200	40	342
Microsemi	MSC040SMA120B	3rd	2018	4.25x4.25	18.1	1200	40	360
GeneSiC	G3R75MT12K	3rd	2010	3.55x2.75	9.76	1200	75	342
onsemi	NVHL080N120SC1	3rd	2010	3.25x2.45	7.96	1200	40	318
onsemi	NTH4L022N120M3S	4th	2012	3.25x2.45	7.96	1200	25	200



The specific per area ON resistance RONxA index of onsemi's NTH4L022N120M3S product (see last column of table) is what we would be expected from a fourth-generation SiC MOSFET.

1-2. SiC MOSFET Die

Whole die area, A
 Active area
 Transistor area, AA

【Top Metal】

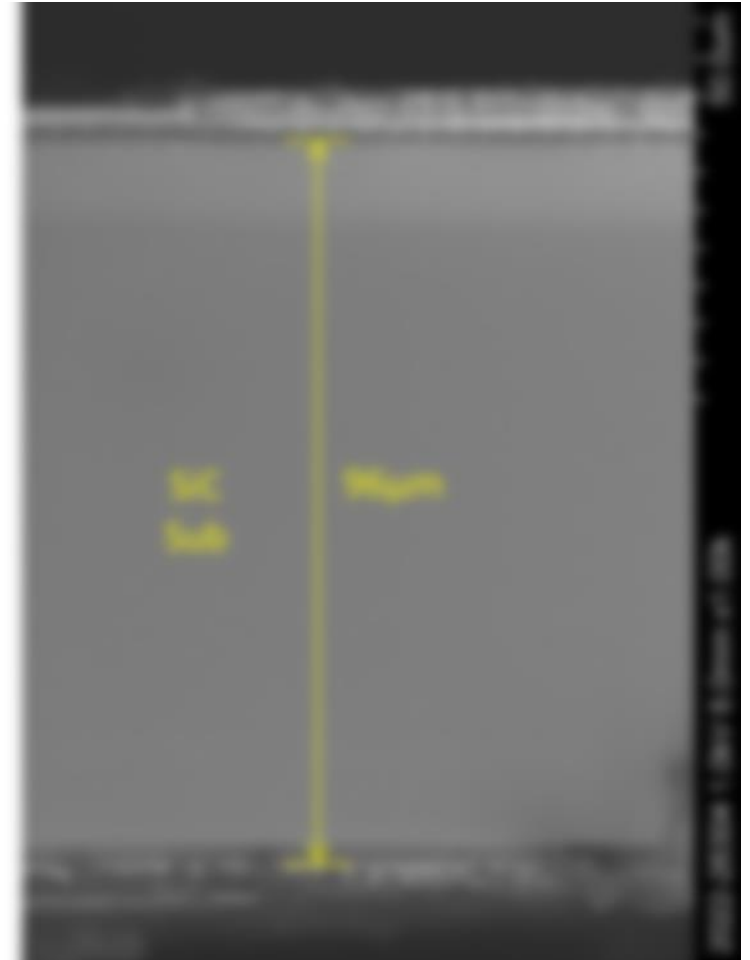
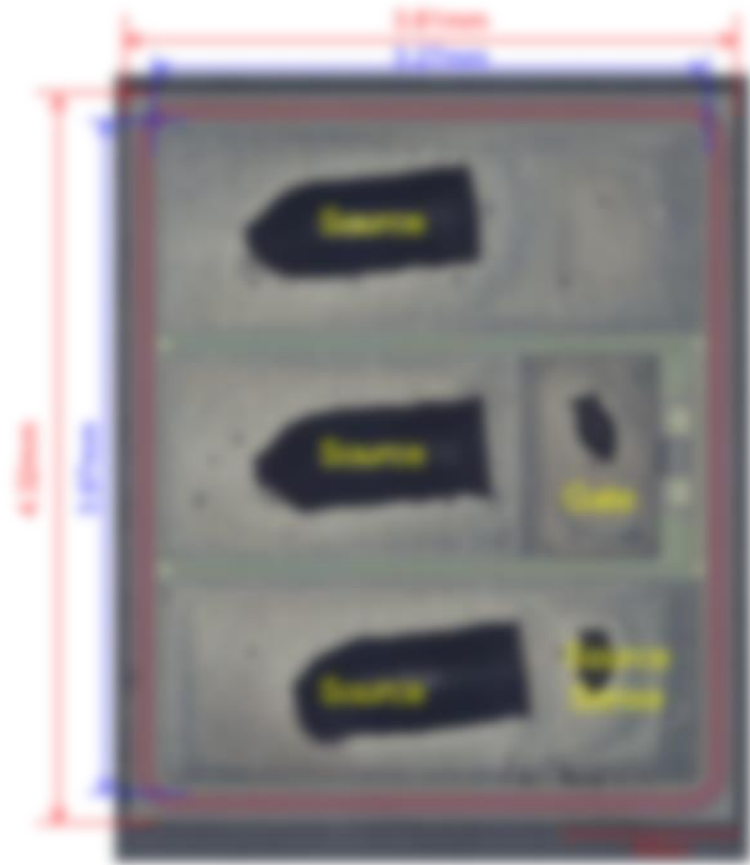


Fig. 1-2-1 Overall image of the SiC MOSFET die

Fig.1-2-2 SiC die thickness

1-3 Transistor array and die edge configuration

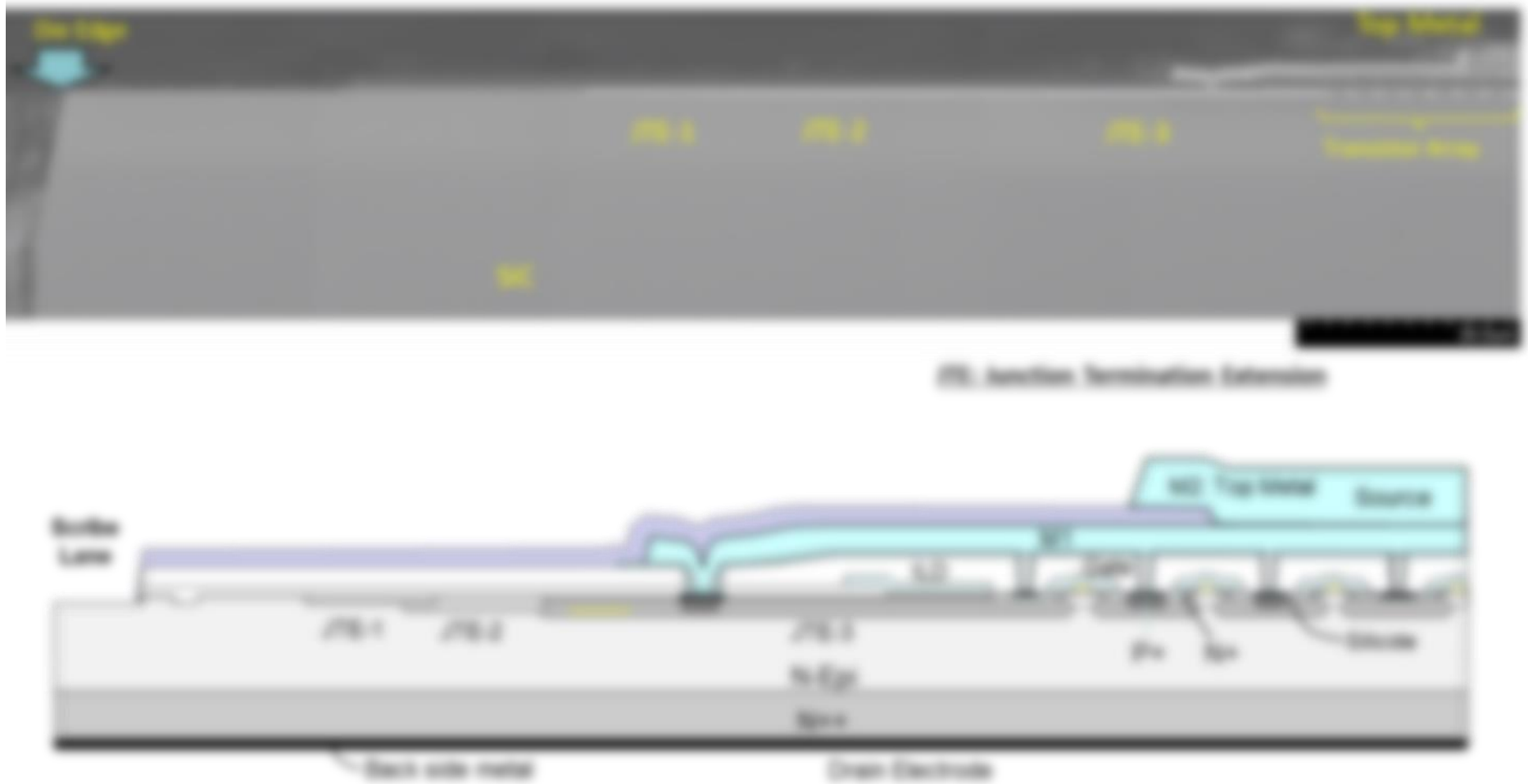


Fig. 1-3-1 Die periphery cross-sectional SEM image

Notes:

- (1) The edge uses Junction Termination Extension (JTE) structure.
- (2) LTPMOS-02B describes a stepped surface in the JTE region, which is formed by etching after JTE 2 ion implantation to adjust/control the JTE charge, but this etching method requires precision JTE charge control by ion implantation dose is considered a better method.

1-4. SiC MOSFET Transistor Cell Structure

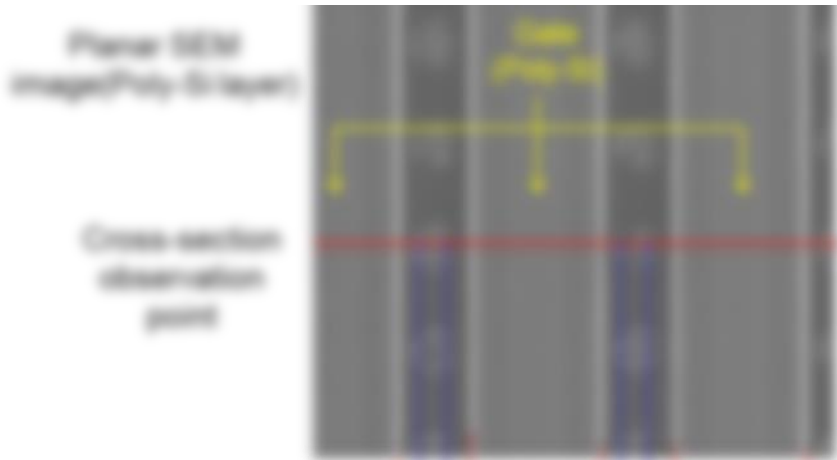


Fig.1-4-1 SiC MOSFET cell array

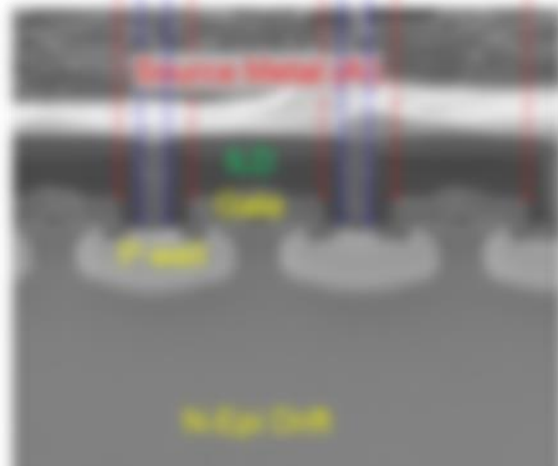
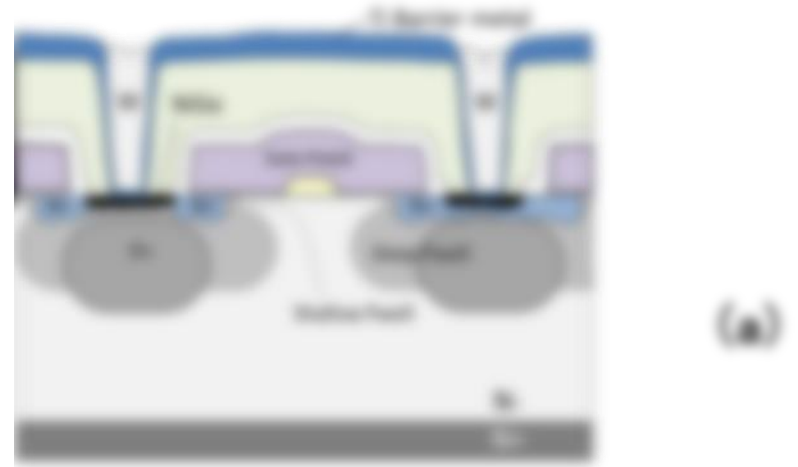
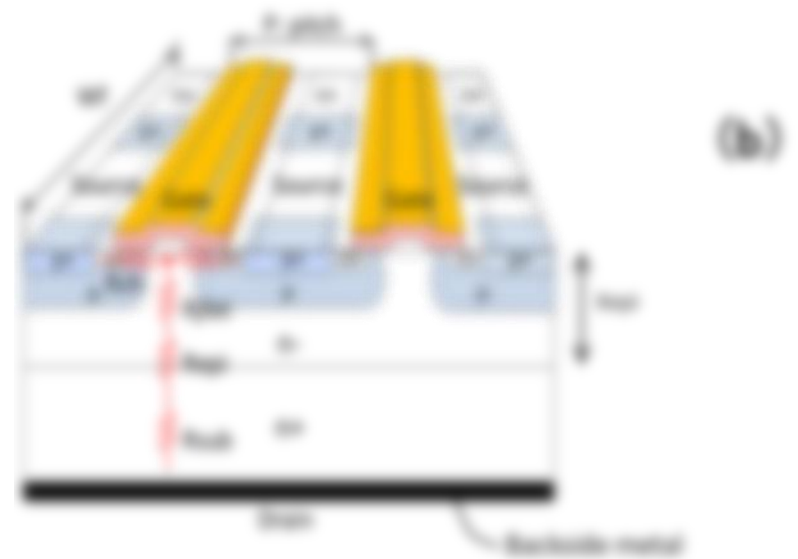


Fig.1-4-2 SiC MOSFET cell Cross-section SEM image



(a)



(b)

Fig.1-4-3 (a) SiC MOSFET cell (b) Schematic diagram of SiC MOSFET array structure

1-5. Metallization (M1 and M2) and gate pad on active area

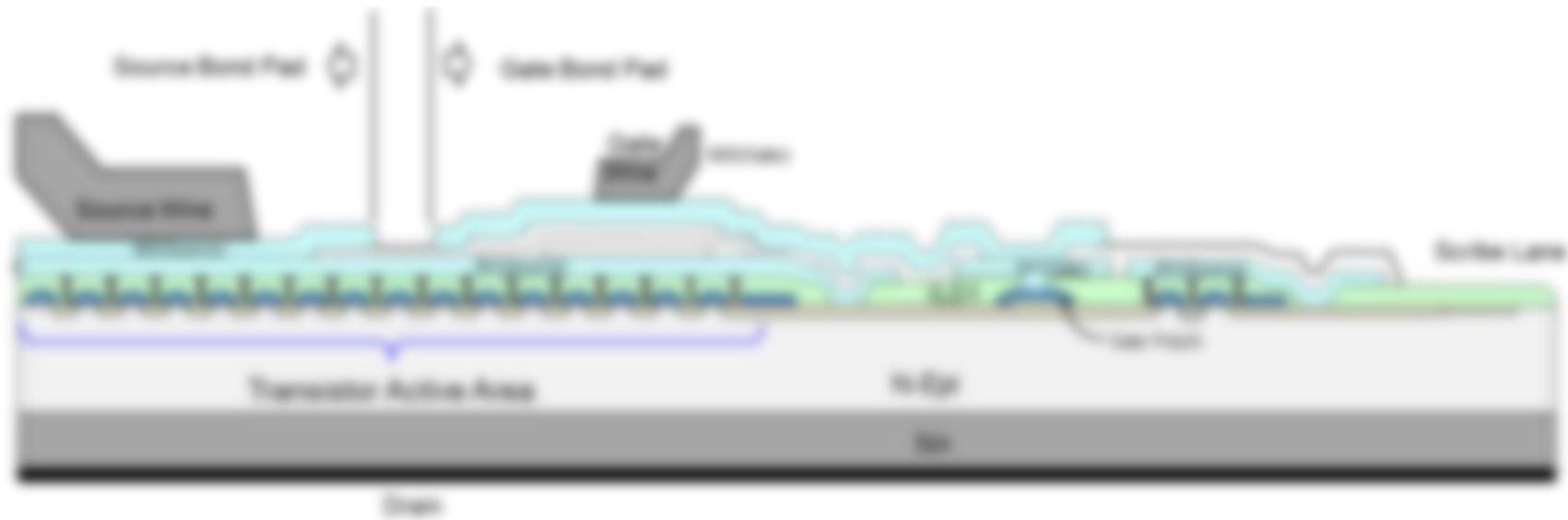
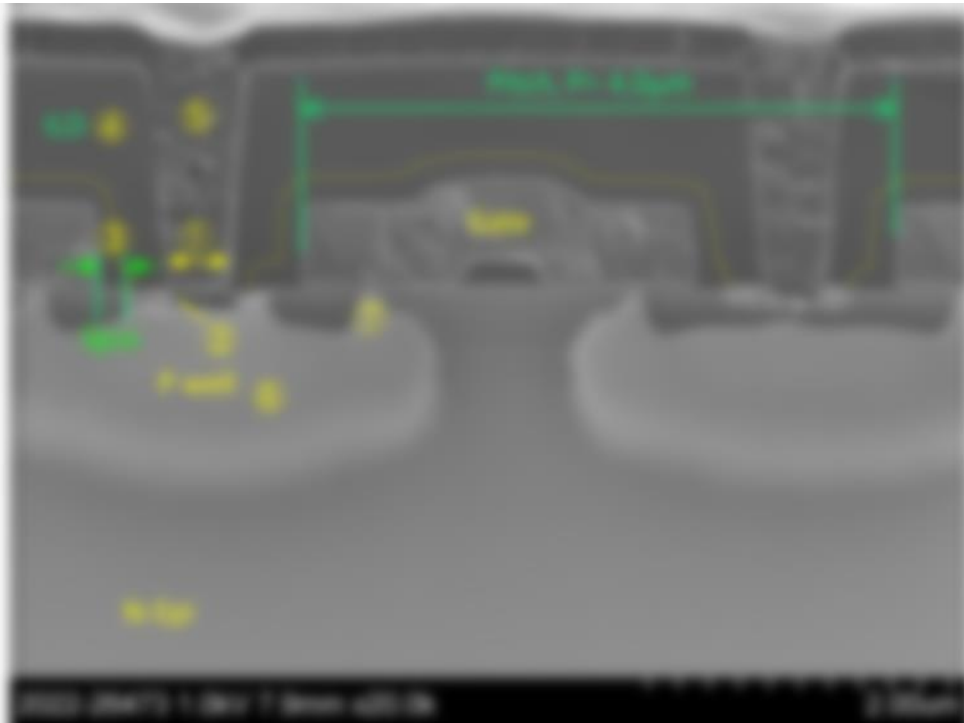


Fig. 1-5-1 Detail of 2-layer metal routing (M1 and M2) and configuration of M2 gate pad on active area of transistor

2. SiC MOSFET Observation

2-1. Transistor structure and process features (1)



- ① 10 μm gate contact opening
- ② Thin oxide layer with a dedicated mask.
Requires thin SiO₂ (PECVD)
- ③ Thin mask and gate trench opening (gap 0.2 μm), the alignment accuracy is strict.
- ④ SiO₂ for surface flattening (PECVD)
- ⑤ W-etchback contact
- ⑥ Multi-ion implant (Pwell) is used.
- ⑦ Channel length (ch-ld) is 10 μm. → Self-aligned formation requires precise control of CVD side wall thickness.

Using an i-line stepper (248nm & 325nm equivalent), the photolithography process requirements are believed to be met.

Fig. 2-1-1 Transistor cell cross-section SEM image

2-1. Transistor structure and process features (8)

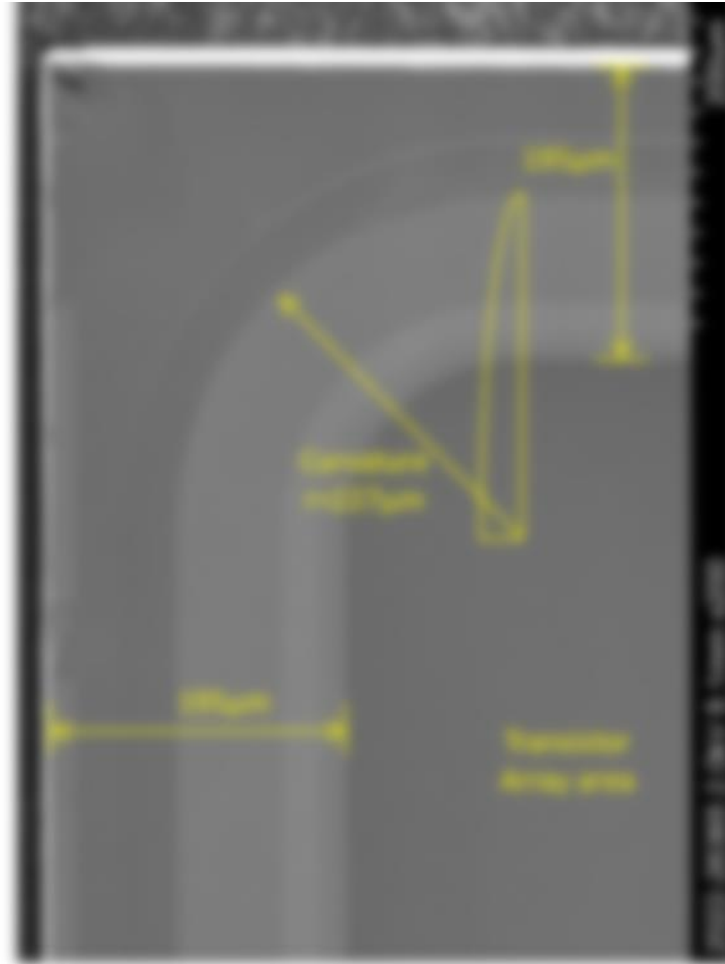


Fig. 2-1-25 Phase SEM image of the die outer periphery

The die edge termination (die edge) uses a P-well extension (PWE) to reduce the electric field strength. The PWE is electrically connected to the source terminal of the transistor. A three-region PWE structure is formed, requiring three masking and ion-implantation steps.

2-2. Details of self-alignment process of N+ and P-well implants to determine channel length Lch



Fig. 2-2-1 Key features of the M3S transistor structure

3. SiC MOSFET NTH4L022N120M3S Analysis Results Summary

Table 3-1: Device structure: SiC MOSFET

Die size	mm	mm	Figure 3-1
Die area, A	mm ²	mm ²	Figure 3-1
Die active area	mm ²	mm ²	Figure 3-1
Transistor Active area, AA	mm ²	mm ²	Figure 3-1
Transistor peripheral width (Uneffective)	mm	mm	Figure 3-1
N Epi (Drift) thickness, Xepi	mm	mm	Figure 3-1
Transistor cell configuration	Figure 3-1		Figure 3-1
Transistor cell basic structure (Gate)	Figure 3-1		Figure 3-1
P-Well depth/width, Xp/a	mm	mm	Figure 3-1
Cell Source/Source pitch, P	mm	mm	Figure 3-1
MOSFET Channel Length, Lch	mm	mm	Figure 3-1
MOSFET Gate electrode width, Wg	mm	mm	Figure 3-1
Total Channel width, W	mm	mm	Figure 3-1
ON Resistance, RON	mΩ	Ω	Specified
Intrinsic RON x A (Transistor AA)	mΩ·mm ²	Ω·mm ²	This value is comparable to the 4th generation SiC MOSFET devices of other manufacturers.
Effective RON x A (Die area, A)	mΩ·mm ²	Ω·mm ²	

Table 3-2: SiC MOSFET structure: Layers materials and thicknesses

Description	Layer thickness	Material	Properties
Wafer type/configuration (Bulk, Epi)	1000 μm 1200 μm	SiC	Crystal orientation: Not indicated F 10, Fig. 2-1-1
N-epi (Drift)	8 μm	SiC	F 10, Fig. 2-1-1: Estimated from 100-potential control Doping: doping concentration is 4e17 cm ⁻³ (approx.) F 10, Fig. 2-1-1
N Buffer layer	1.5 μm (1 μm)	SiC	F 10, Fig. 2-1-1: Estimated from 100-potential control F 10, Fig. 2-1-1
P well depth	1 μm	SiC	F 10, Fig. 2-1-1: Estimated from 100-potential control
N+ depth	100 nm	SiC	Refer to the structure analysis report (22G-0037-2)
Gate electrode structure	1 μm	Al ₂ O ₃	Refer to the structure analysis report (22G-0037-2)
Gate dielectric	100 nm	Aluminum nitride	Refer to the structure analysis report (22G-0037-2)
Field oxide	1 μm	SiO ₂	Refer to the structure analysis report (22G-0037-2)
Silicide layer	100 nm	SiC	F 10, Fig. 2-1-1
Source barrier metal (M1)	40-100 nm	TiAlN	Refer to the structure analysis report (22G-0037-2)
Source metal (M1)	1 μm	Al ₂ O ₃	F 10, Fig. 2-1-1
Source barrier metal (M2)	100 nm	TiAlN	Refer to the structure analysis report (22G-0037-2)
Source metal (M2)	1 μm	Al ₂ O ₃	F 10, Fig. 2-1-1
ILD1 (Gate-M1)	1.1 μm	SiO ₂	Refer to the structure analysis report (22G-0037-2)
ILD2 (M1-M2)	1.1 μm	SiO ₂	F 10, Fig. 2-1-1 F 10, Fig. 2-1-1: The ILD between M1 and M2 is formed with TiAlN. Details on page 10
Protection layer	Not indicated	SiO ₂	Not indicated
Die back-side metal	1000 μm	SiC	Refer to the structure analysis report (22G-0037-2)

4. Process Flow

4-1. SiC MOSFET front-end wafer process flow (Estimated)

Based on (a) layer structure, (b) cross section and (c) EDX material analyses shown in the report of 22G-0037-1, the following device manufacturing process sequence is estimated. Rather than extracting the detailed process flow, it is an object to recognize the structure/layer of a device for accurate analysis.

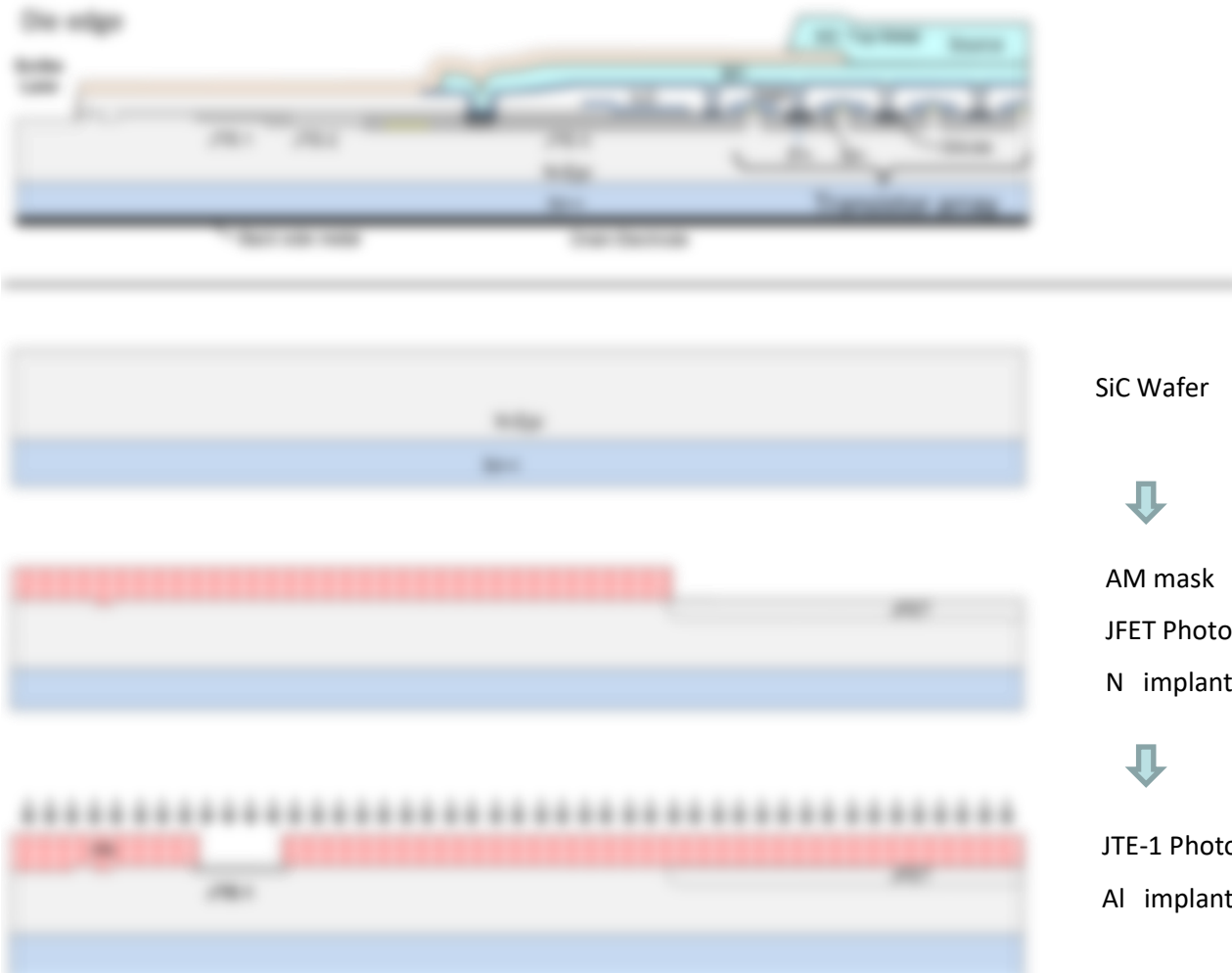
onsemi SiC MOSFET NTH4L022N120M3S process flow sequence

Mask	Process	Comment
	Wafer	
[1]	AM Photo Oxide	
[2]	JFET Photo N implant	
[3]	JTE1 Photomask JTE1 implant Al/B ions	
[4]	JTE2 Photomask JTE2 implant Al/B ions CVD Oxide deposition PolySi deposition PolySi etching	
[5]	PW1 (Hardmask) Photo PolySi + CVDOx etch Pwell-1 implant Al/B ions Pwell-2 implant inclined Al/B ions CVDoxide deposition (SW) CVDoxide etchback Screening oxide growth	
[6]	N+ Photo N+ ion implant	
[7]	PW2 Photo Pwell-3 implant Al/B ions P+ implant: Al ions Remove Sidewall oxide Hard Mask CVDoxide etch Remove PolySi mask Capping layer deposition Annealing Remove Capping layer PECVD oxide deposition	
[8]	FOX Photo Oxide etch Remove FOX mask Gate Oxide PolySi Depo/doping	

Mask	Process	Comment
[9]	GP (Gate Poly) Photomask PolySi etch PECVD oxide deposition	
[10]	SO (Silicide) Photo PECVD etching Silicide metal Sputter Silicidation ILD1 (B)PSG deposition Reflow melting	
[11]	CO (Contact) Photo CO ILD etching Al Metal deposition	
[12]	M1 (Metal) Photo Metal etching ILD2a CVD oxide deposition	
[13]	VHA Photo ILD2a etching ILD2b CVD oxide deposition	
[14]	VHB Photo ILD2b etching ILD2c CVD oxide deposition	
[15]	VIA Photo ILD etching Al-2 Metal deposition	
[16]	M2 (Metal) Photo Metal etching Passivation layer deposition	
[17]	BW (Bonding Window) Photo Passivation layer etching Wafer backside grinding Backside metal deposition Dicing (singulation)	

• It is estimated that 17 photo/masking steps are used for the front-end process up to the backside metallization process.

Process sequence of onsemi NTH4L022N120M3S SiC MOSFET (estimated) (1)



5. Device structure and electrical characteristics analysis

In this section the measurement results of the following electrical characteristics are analyzed.

1. Id-Vds characteristics
2. Off-State drain current Idss vs. drain voltage (Vds) with device temperature as parameter, and activation energy (Ea)
3. Off-state breakdown voltage BVdss characteristics and operation margin
4. Leakage current comparison between SiC MOSFETs manufacturers
5. Body diode characteristics
6. Capacitances (Ciss, Coss, Crss)-Vds characteristics

Furthermore, the correlation between the electrical characteristics and the physical structure of the transistor is considered,

7. Device structure and electrical characteristics analysis: ON resistance
8. N-Epi layer impurity concentration analysis

The data presented in this section do not represent a wide range of statistical samples but can still be considered as reference values. In addition, it is worth noting that systematic and regular evaluations should be considered as manufacturers are constantly striving to improve the manufacturing process for SiC wafers and epilayers.

5-1. SiC MOSFET NTH4L022N120M3S Id-Vds characteritics

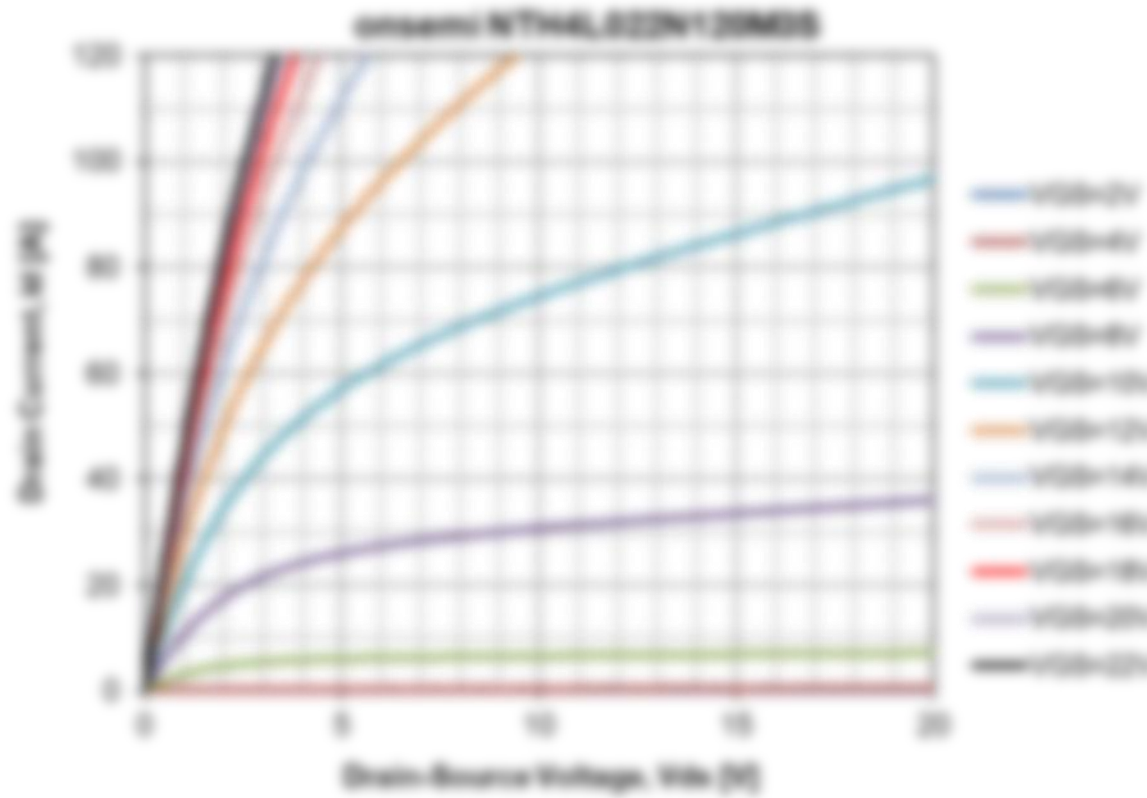


Fig. 5-1-1 SiC MOSFET Id-Vds characteristics

The extracted DC on-resistance from the Id-Vds characteristics is $R_{DS(on)} = 22\text{ m}\Omega$ (data sheet 22mΩ (typical)), measured under the conditions of $V_{gs} = 18\text{V}$ and $I_D = 40\text{A}$.

5-2. Off-State drain current I_{dss} vs. drain voltage (V_{ds}) and activation energy (E_a)

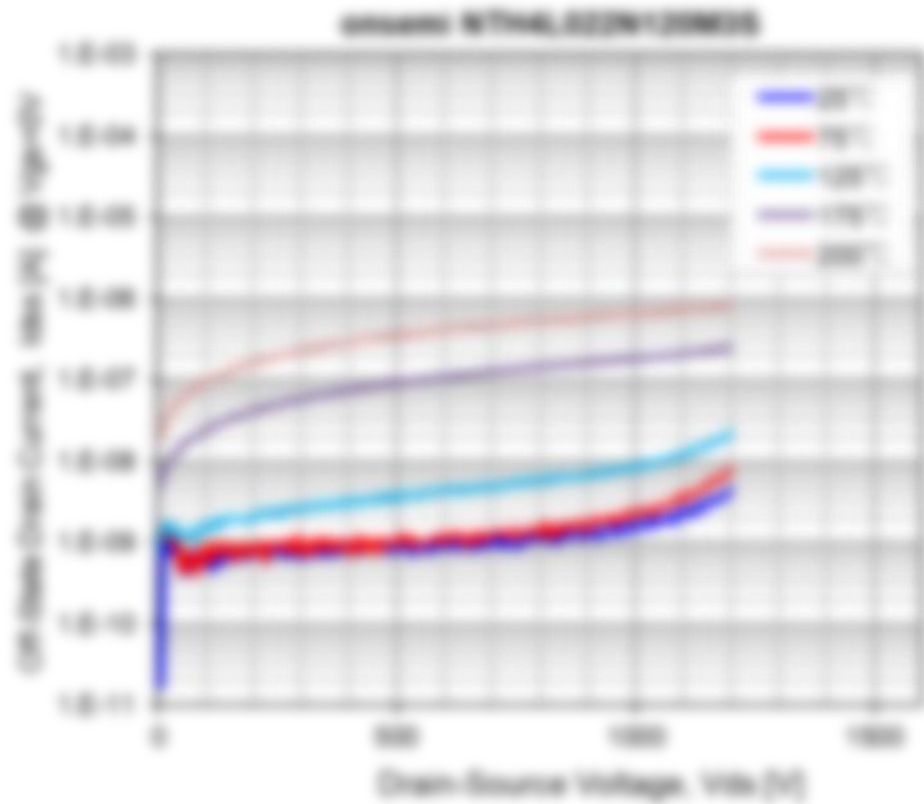


Fig. 5.2.1 Off-state I_{dss} vs. V_{ds} characteristics with device temperature as a parameter

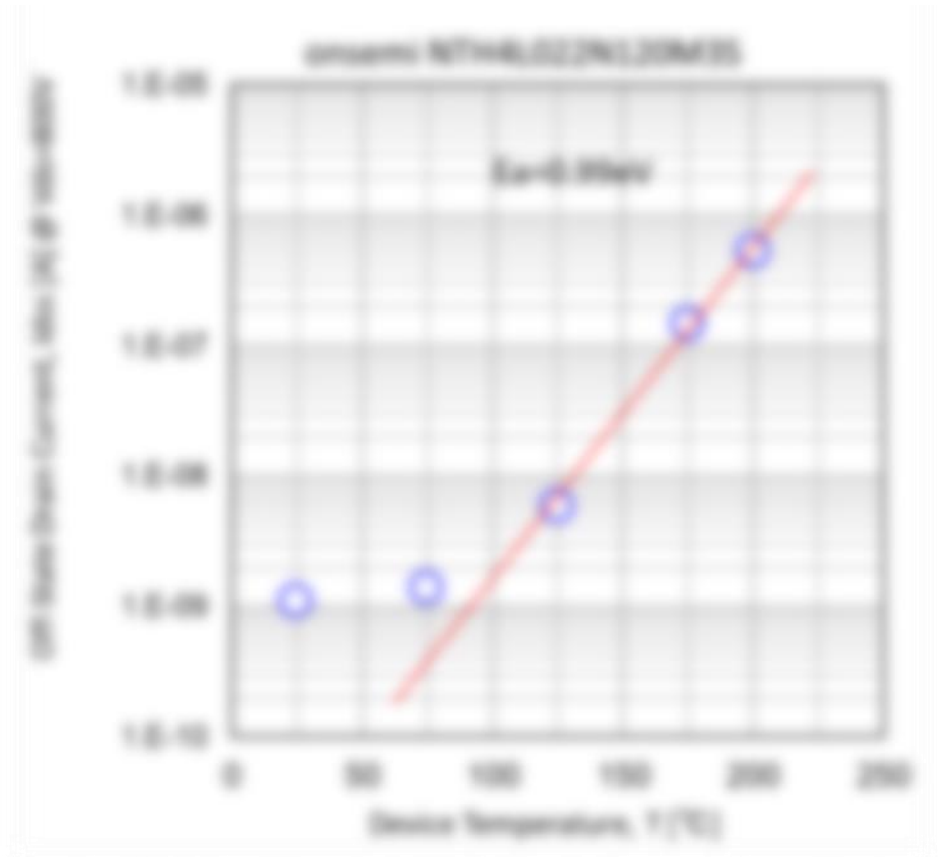


Fig. 5.2.2 Temperature dependence of off-state drain current at $V_{ds} = 800\text{V}$

The drain leakage current I_{dss} begins to rise from 50V . The activation energy extracted at $V_{ds} = 800\text{V}$ is $E_a = 0.38 \text{ eV}$.

The on-resistance components are estimated by analysis of the measured I_d - V_{ds} - V_{gs} characteristics and device structure data.

- 1) R_{ch} accounts for about 45% of R_{on} .
- 2) The thick SiC substrate resistance, R_{sub} accounts for about 8% of R_{on} .

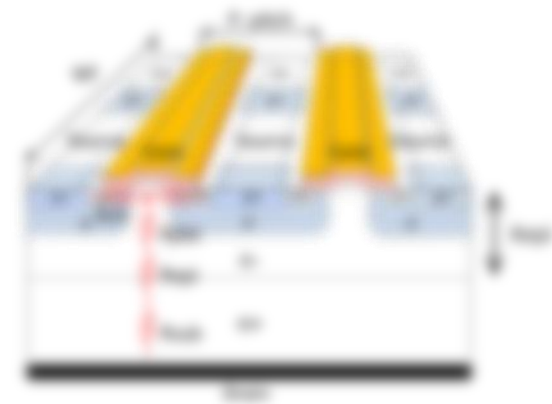
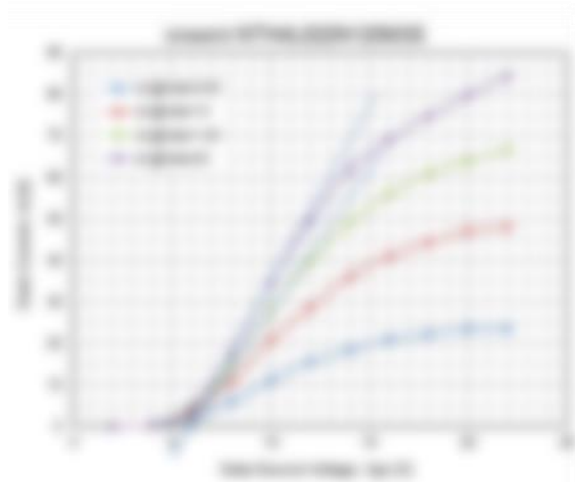
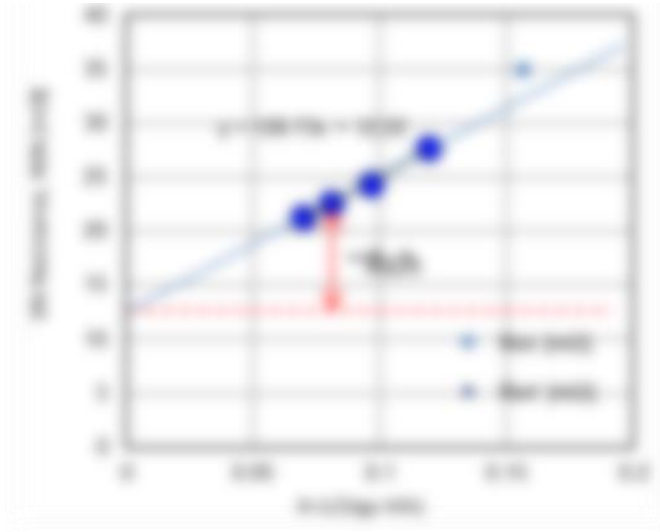
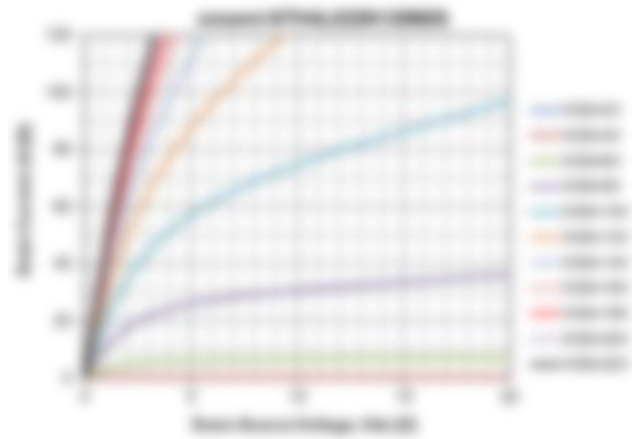


Fig. 5-7-1 SiC MOSFET Characteristics for RON Analysis

6. Related references

(1) ON Semiconductor, "NTH4L022N120M3S MOSFET Datasheet", January, 2022 - Rev. 4
<https://www.onsemi.com/pdf/datasheet/nth4l022n120m3s-4.pdf>

7. Related patents

(1) US 10,621,228 B2: SiC power device having a high voltage termination
(2) US 10,621,229 B2: SiC power device having a high voltage termination
(3) US 10,621,230 B2: Configuration of portions of a power device within a SiC crystal

United States Patent		Patent No. 10,948,100 B2	
Application		Date of Patent: Dec. 8, 2020	
Inventors:		Assignee:	
Attorney:		IPC Class.:	
Abstract:		References:	
Claims:		Notes:	
Drawings:		Examiner:	
Publication:		Agency:	
Priority:		Related:	
Filed:		Examined:	
Pub. No.:		Pub. Date:	
Pub. No.:		Pub. Date:	

(7) ABSTRACT

In one general aspect, an apparatus can include a semiconductor region including a silicon carbide material and a junction termination extension implant region disposed in the semiconductor region. The apparatus can include a low interface state density portion of a dielectric layer having at least a portion in contact with the junction termination extension implant region.

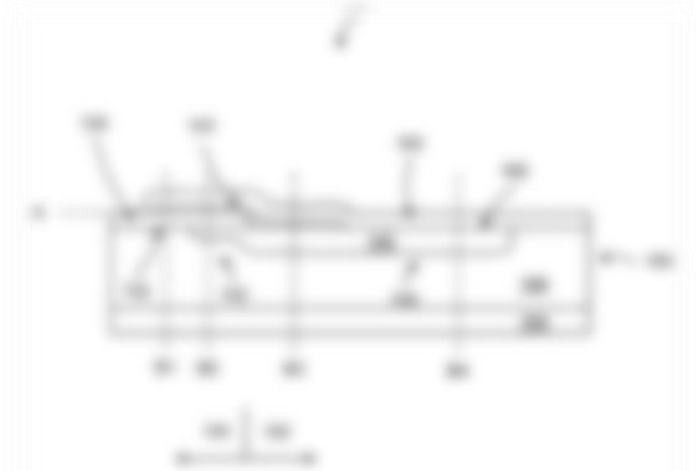


FIG. 1



FIG. 2

Junction Termination Extension (JTE) related patent