Mar 23, 2023

Product Analysis Report

No.22G-0037-2 Onsemi NTH4L022N120M3S Process and Electrical Characteristics Analysis

Product	: SiC MOSFET
Part No.	: NTH4L022N120M3S
Manufacturer	: ON Semiconductor Corporation
Die size	: SiC MOSFET
Process	: SiC wafer, Planer Gate, Top Metal Source, Double metal process

This report is a process flow analysis report based on the structure analysis results of Report 22G-0018-1, and it includes the following contents,

I. Estimating process manufacturing sequence of SiC MOSFET and photo/masking process steps

II. Considerations on the main process features.

III. Doping concentration profile analysis of the extracted N-epi layer.

IV. Correlation between device structure and electrical characteristics.

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Content		Page
1	Onsemi's SiC MOSFET NTH4L022N120M3S : Summary of analysis results	3
1-1.	Comparison of characteristics between onsemi M3S and other companies' SiC MOSFETs	4
1-2.	SiC MOSFET Die	5
1-3	Transistor array and die edge configuration	6
1-4	SiC MOSFET Transistor Cell Structure	7
	Schematic diagram of whole die cross section and schematic layout pattern	
1-5	Metallization (M1 and M2) and gate pad on active area	8
2	SiC MOSFET Observation	
2-1.	Transistor structure and process features (1)-(8)	9-16
2-2	Details of self-alignment process of N+ and P-well implants to determine channel length Lch	17
2-3	Details of the Side-wall/Screening Oxidation process and the final gate dielectric (oxidation) forming a "stepped" surface.....................	18
3	SiC MOSFET NTH4L022N120M3S analysis result summary...........	
	Table 3-1: Device structure, SiC MOSFET	19
	Table 3-2: Device structure, Layers material and thicknesses	20

Content		Page
4	Process Flow	
4-1.	SiC MOSFET front-end wafer process flow (Estimated)	21
4-2.	SiC MOSFET process sequence cross section schematics	22-26
5	Device structure and electrical characteristics analysis	27
5-1.	SiC MOSFET NTH4L022N120M3S Id-Vds characteritics........	28
5-2.	Off-State drain current Idss vs. drain voltage (Vds) and activation energy (Ea)	29
5-3.	Off-state breakdown voltage BVdss characteristics	30
5-4.	Leakage current comparison between SiC MOSFETs manufacturers	31
5-5.	Body diode characteristics	32
5-6.	Capacitances (Ciss, Coss, Crss)-Vds characteristics	33
5-7.	Device structure and electrical characteristics analysis: ON resistance	34
5-8.	N-Epi layer impurity concentration analysis	36
5-9.	Device structure and electrical characteristics analysis: Breakdown voltage	37
6	Related references	38
7	Related patents	38

1. Onsemi's SiC MOSFET NTH4L022N120M3S: Summary of analysis results

1-1. Comparison of characteristics between onsemi M3S and other companies' SiC MOSFETs.

Maker	Part no.	Process Gen	Production	Die Size mmxmm	Die Size mm2	Vdss [V]	RON [mΩ]	Intrinsic RONxA [mΩ·mm^2]
ROHM	SCT2080KE	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
ROHM	SCT3080KL	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
ROHM	SCT4062KR	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
WOLFSPEED (CREE)	C3M0075120K	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
INFINEON	AIMW120R060M1H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Microsemi	MSC040SMA120B	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
GeneSiC	G3R75MT12K	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
onsemi	NVHL080N120SC1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
onsemi	NTH4L022N120M3S	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

The specific per area ON resistance RONxA index of onsemi's NTH4L022N120M3S product (see last column of table) is what we would be expected from a fourth-generation SiC MOSFET.

1-2. SiC MOSFET Die

Whole die area, A	[illegible]
Active area	[illegible]
Transistor area, AA	[illegible]

【Top Metal】

Fig. 1-2-1 Overall image of the SiC MOSFET die

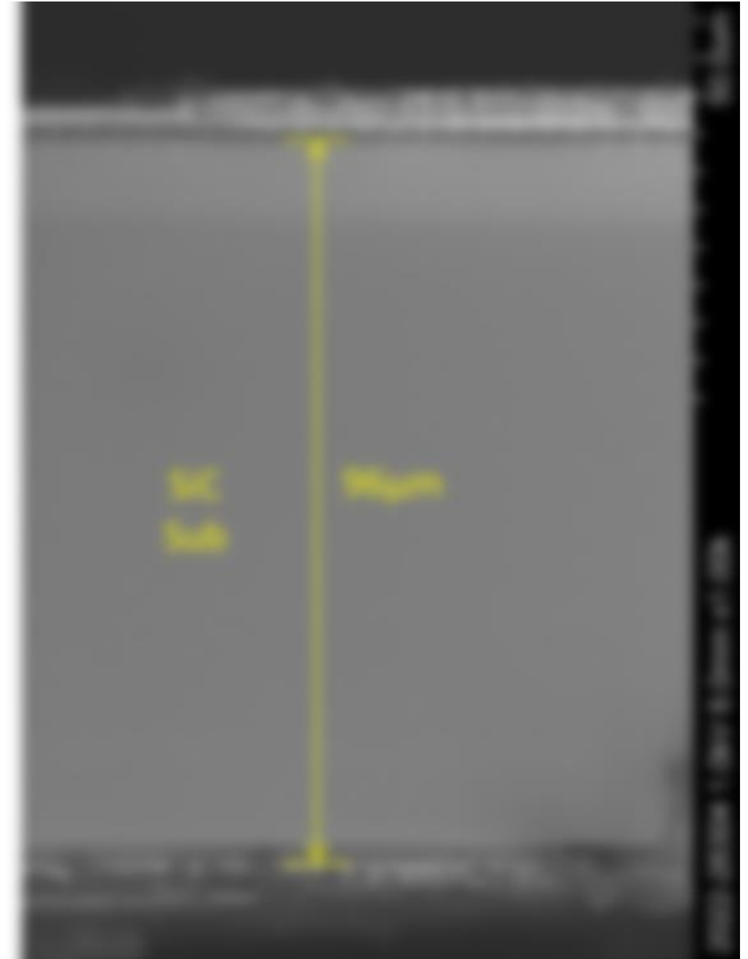


Fig.1-2-2 SiC die thickness

1-3 Transistor array and die edge configuration

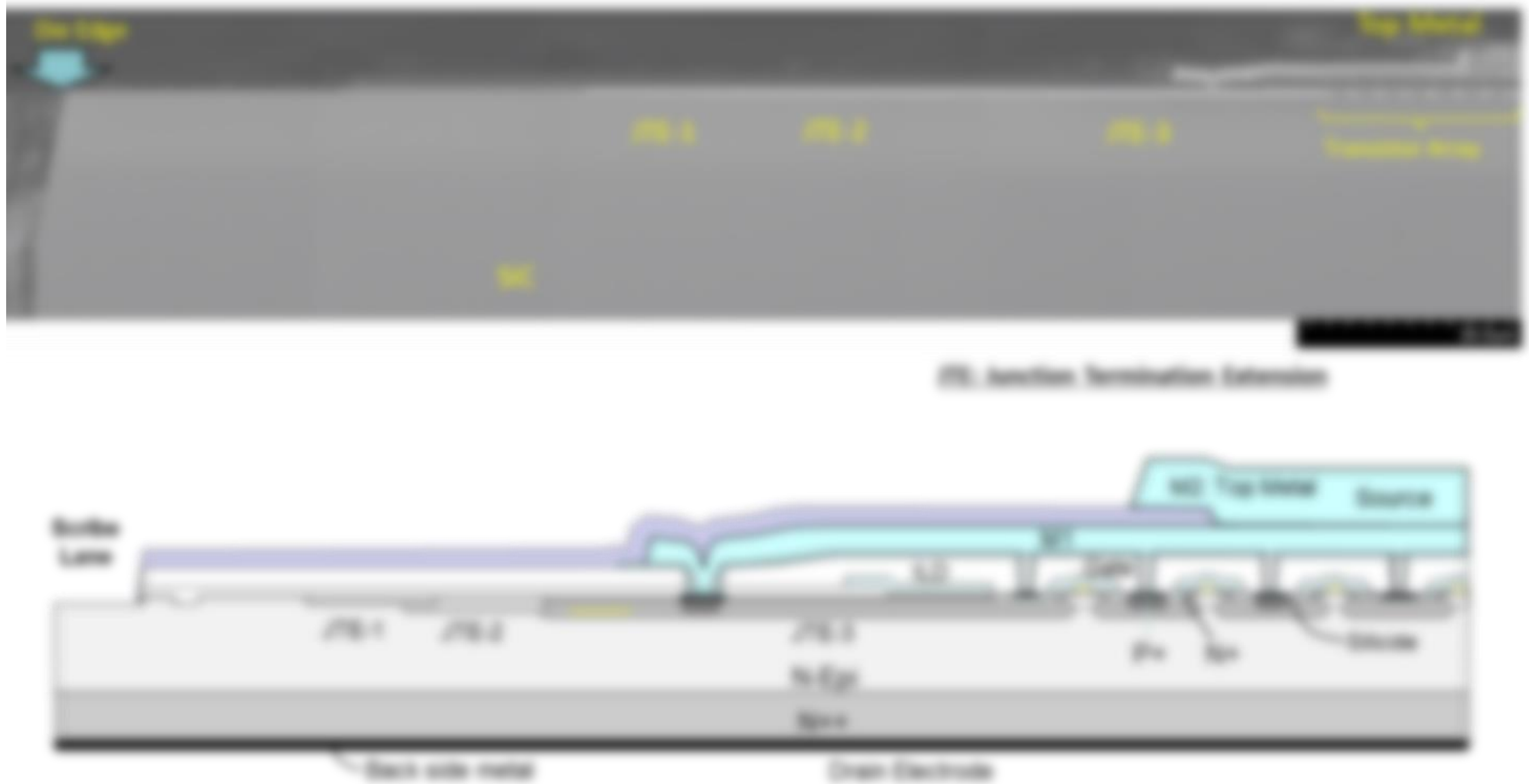


Fig. 1-3-1 Die periphery cross-sectional SEM image

1-4. SiC MOSFET Transistor Cell Structure

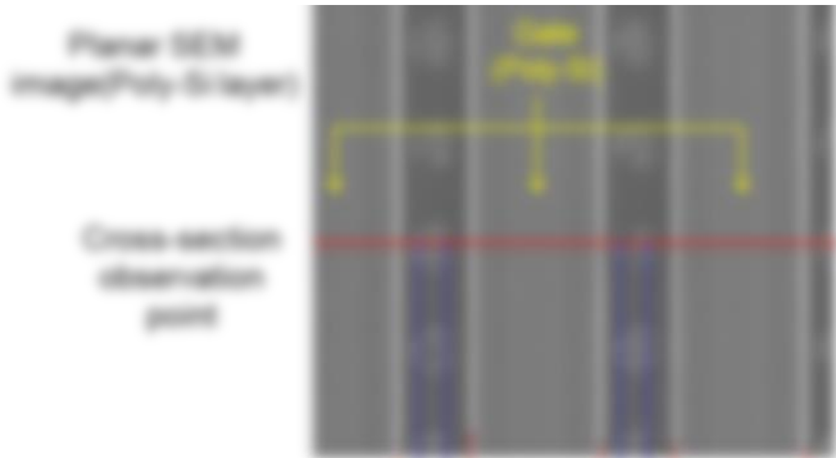


Fig.1-4-1 SiC MOSFET cell array

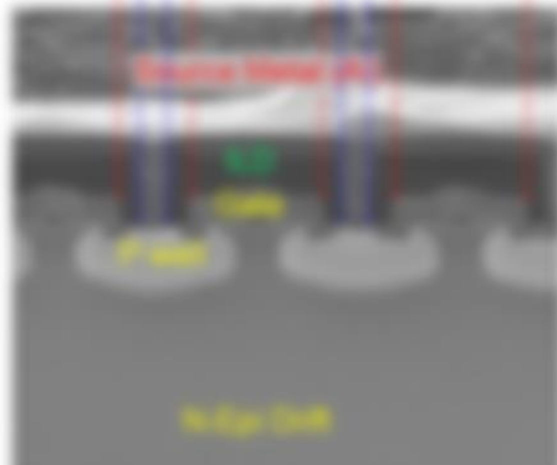
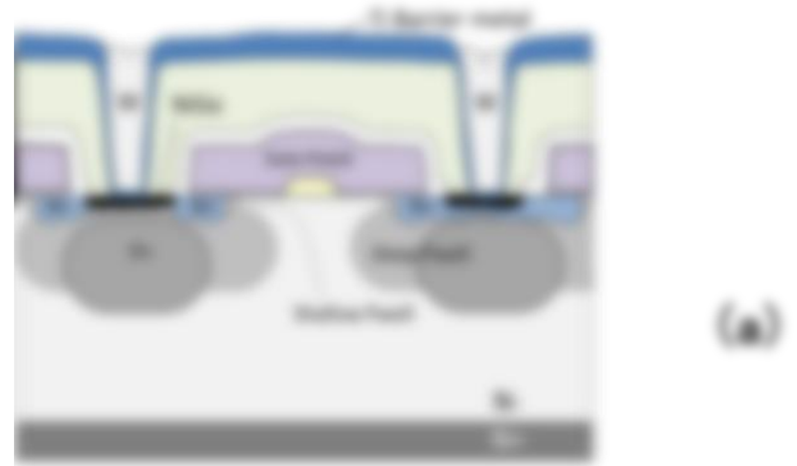


Fig.1-4-2 SiC MOSFET cell Cross-section SEM image



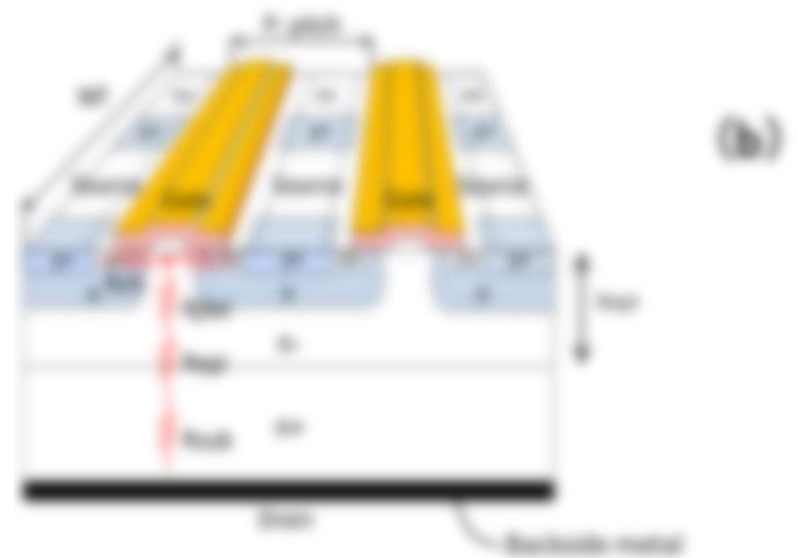


Fig.1-4-3 (a) SiC MOSFET cell (b) Schematic diagram of SiC MOSFET array structure

1-5. Metallization (M1 and M2) and gate pad on active area

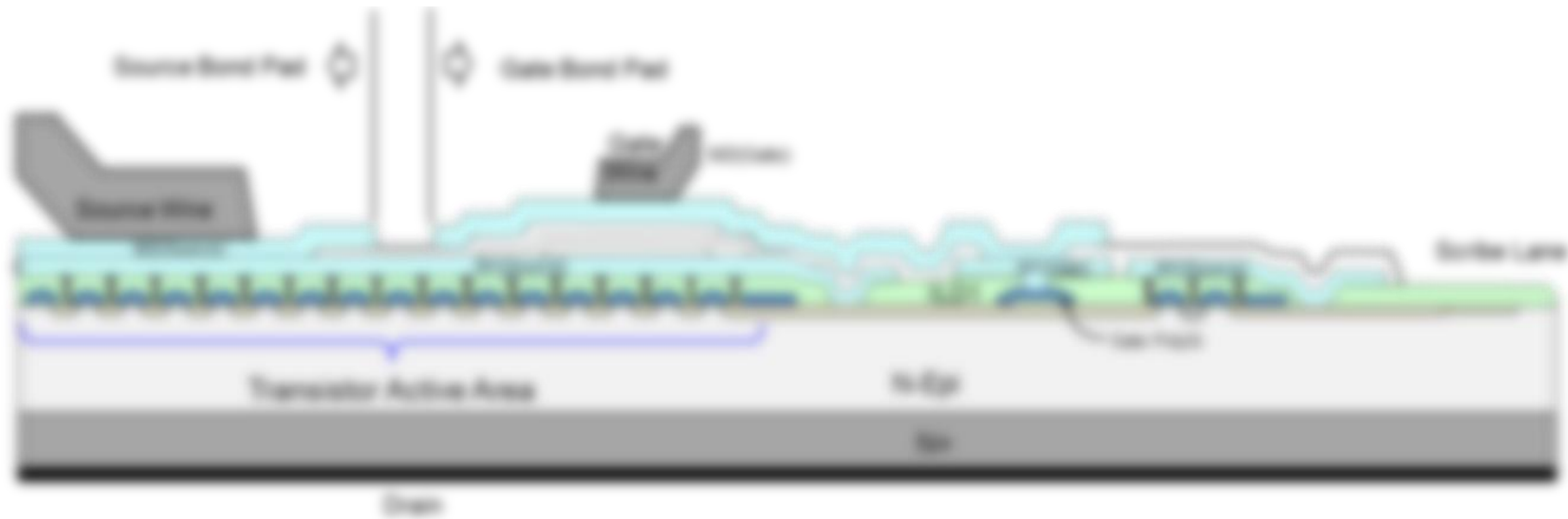


Fig. 1-5-1 Detail of 2-layer metal routing (M1 and M2) and configuration of M2 gate pad on active area of transistor

2. SiC MOSFET Observation

2-1. Transistor structure and process features (1)

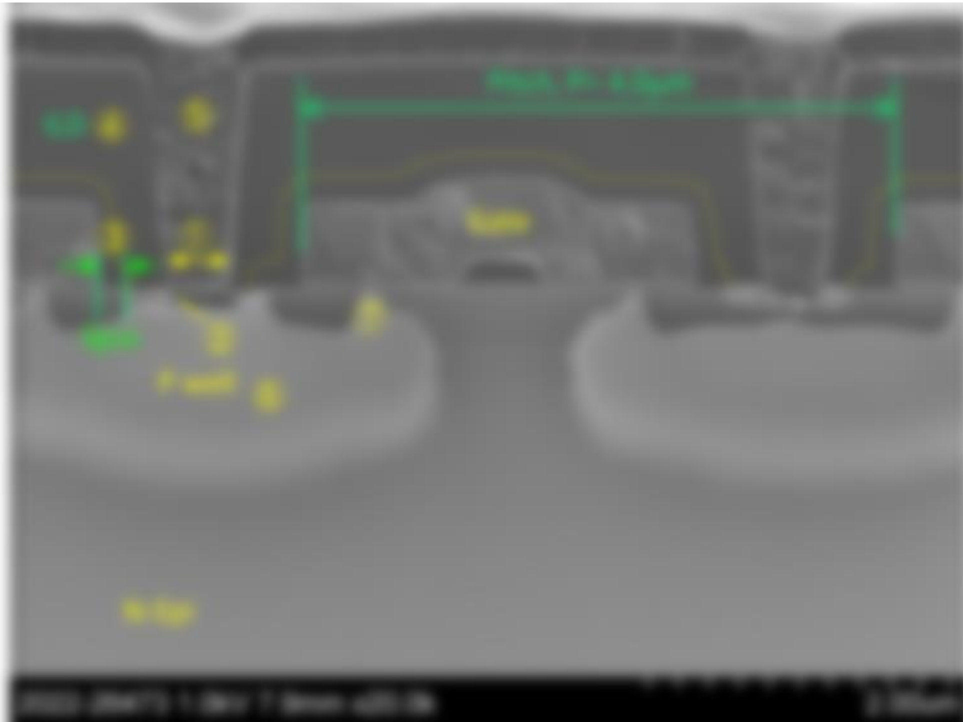
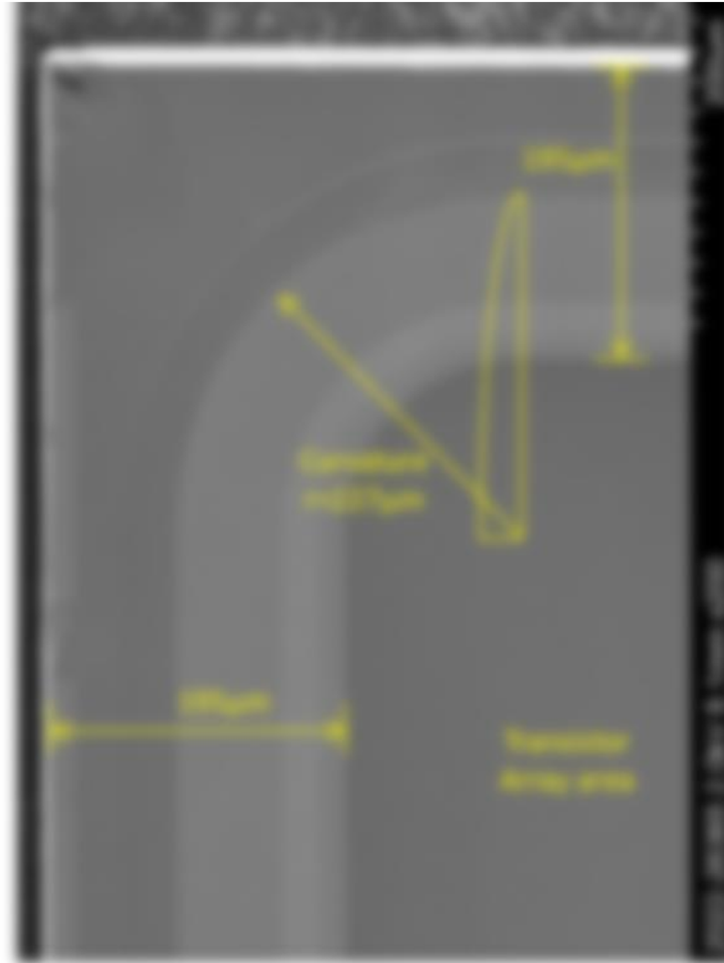


Fig. 2-1-1 Transistor cell cross-section SEM image

2-1. Transistor structure and process features (8)



2-2. Details of self-alignment process of N+ and P-well implants to determine channel length Lch

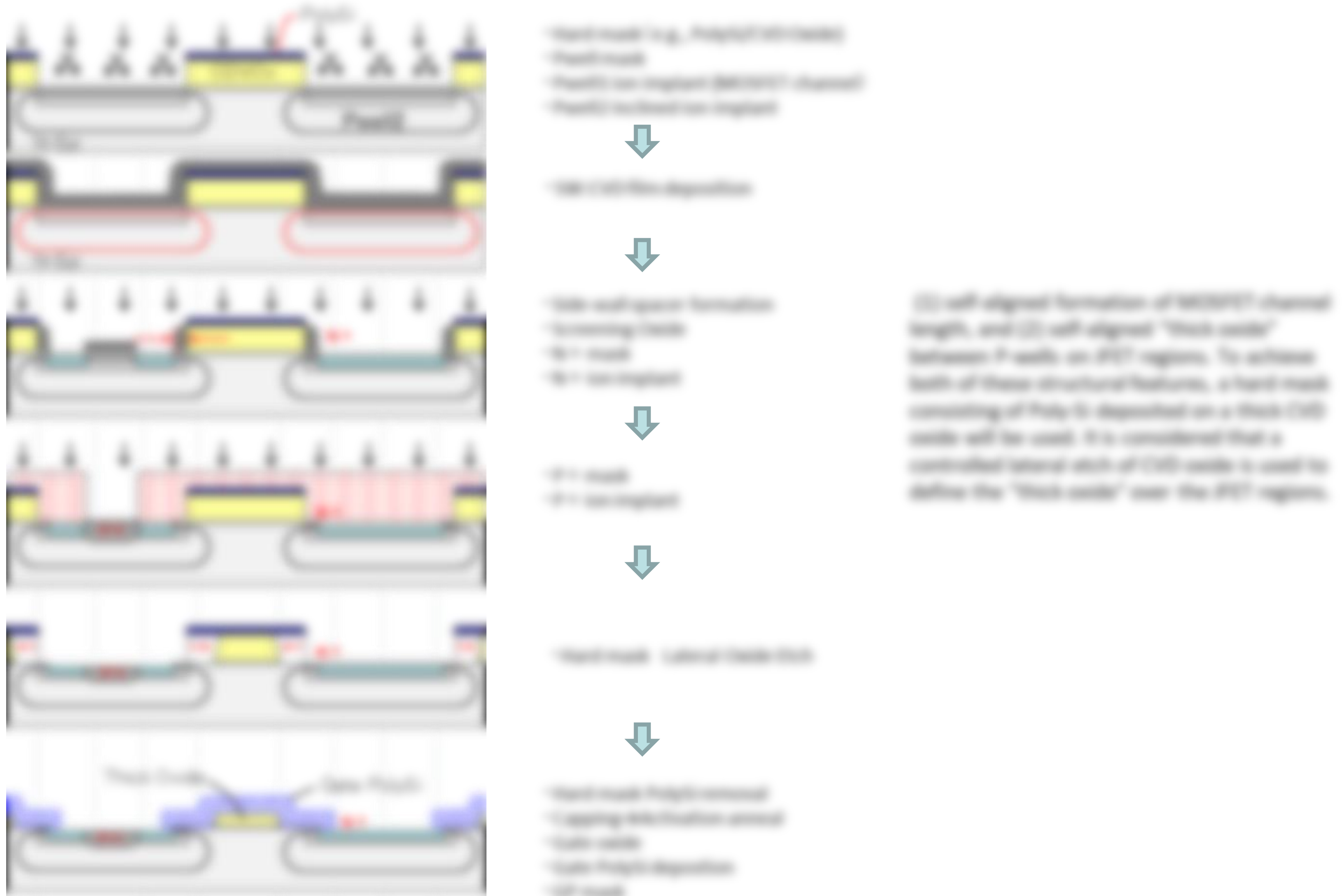


Fig. 2-2-1 Key features of the M3S transistor structure

3. SiC MOSFET NTH4L022N120M3S Analysis Results Summary

Table 3-1: Device structure: SiC MOSFET

Item	Unit	Value	Remarks
Die size	[illegible]	[illegible]	[illegible]
Die area, A	[illegible]	[illegible]	[illegible]
Die active area	[illegible]	[illegible]	[illegible]
Transistor Active area, AA	[illegible]	[illegible]	[illegible]
Transistor peripheral width (Uneffective)	[illegible]	[illegible]	[illegible]
N Epi (Drift) thickness、Xepi	[illegible]	[illegible]	[illegible]
Transistor cell configuration	[illegible]		[illegible]
Transistor cell basic structure (Gate)	[illegible]		[illegible]
P-Well depth/width, Xp/a	[illegible]	[illegible]	[illegible]
Cell Source/Source pitch, P	[illegible]	[illegible]	[illegible]
MOSFET Channel Length, Lch	[illegible]	[illegible]	[illegible]
MOSFET Gate electrode width, Wg	[illegible]	[illegible]	[illegible]
Total Channel width, W	[illegible]	[illegible]	
ON Resistance, RON	[illegible]	[illegible]	[illegible]
Intrinsic RON x A (Transistor AA)	[illegible]	[illegible]	[illegible]
Effective RON x A (Die area, A)	[illegible]	[illegible]	

Table 3-2: SiC MOSFET structure： Layers materials and thicknesses

Description	Layer thickness	Material	Properties
Wafer type/configuration (Bulk, Epi)	[illegible]	[illegible]	[illegible]
N-epi (Drift)	[illegible]	[illegible]	[illegible]
N Buffer layer	[illegible]	[illegible]	[illegible]
P well depth	[illegible]	[illegible]	[illegible]
N+ depth	[illegible]	[illegible]	[illegible]
Gate electrode structure	[illegible]	[illegible]	[illegible]
Gate dielectric	[illegible]	[illegible]	[illegible]
Field oxide	[illegible]	[illegible]	[illegible]
Silicide layer	[illegible]	[illegible]	[illegible]
Source barrier metal（M1）	[illegible]	[illegible]	[illegible]
Source metal (M1)	[illegible]	[illegible]	[illegible]
Source barrier metal（M2）	[illegible]	[illegible]	[illegible]
Source metal (M2)	[illegible]	[illegible]	[illegible]
ILD1 (Gate-M1)	[illegible]	[illegible]	[illegible]
ILD2 (M1・M2)	[illegible]	[illegible]	[illegible]
Protection layer	[illegible]	[illegible]	[illegible]
Die back-side metal	[illegible]	[illegible]	[illegible]

4. Process Flow

4-1. SiC MOSFET front-end wafer process flow (Estimated)

Based on (a) layer structure, (b) cross section and (c) EDX material analyses shown in the report of 22G-0037-1, the following device manufacturing process sequence is estimated. Rather than extracting the detailed process flow, it is an object to recognize the structure/layer of a device for accurate analysis.

onsemi SiC MOSFET NTH4L022N120M3S process flow sequence

Mask	Process	Comment
	Wafer	[illegible]
[1]	AM Photo	[illegible]
	Oxide	[illegible]
[2]	JFET Photo	[illegible]
	N implant	[illegible]
[3]	JTE1 Photomask	[illegible]
	JTE1 implant Al/B ions	
[4]	JTE2 Photomask	[illegible]
	JTE2 implant Al/B ions	
	CVD Oxide deposition	[illegible]
	PolySi deposition	[illegible]
	PolySi etching	
[5]	PW1 (Hardmask) Photo	[illegible]
	PolySi＋CVDOx etch	
	Pwell-1 implant Al/B ions	[illegible]
	Pwell-2 implant inclined Al/B ions	[illegible]
	CVDoxide deposition (SW)	[illegible]
	CVDoxide etchback	[illegible]
	Screening oxide growth	[illegible]
[6]	N+ Photo	[illegible]
	N+ ion implant	
[7]	PW2 Photo	
	Pwell-3 implant Al/B ions	[illegible]
	P+ implant: Al ions	[illegible]
	Remove Sidewall oxide	
	Hard Mask CVDoxide etch	[illegible]
	Remove PolySi mask	
	Capping layer deposition	[illegible]
	Annealing	[illegible]
	Remove Capping layer	
	PECVD oxide deposition	[illegible]
[8]	FOX Photo	[illegible]
	Oxide etch	
	Remove FOX mask	
	Gate Oxide	[illegible]
	PolySi Depo/doping	[illegible]

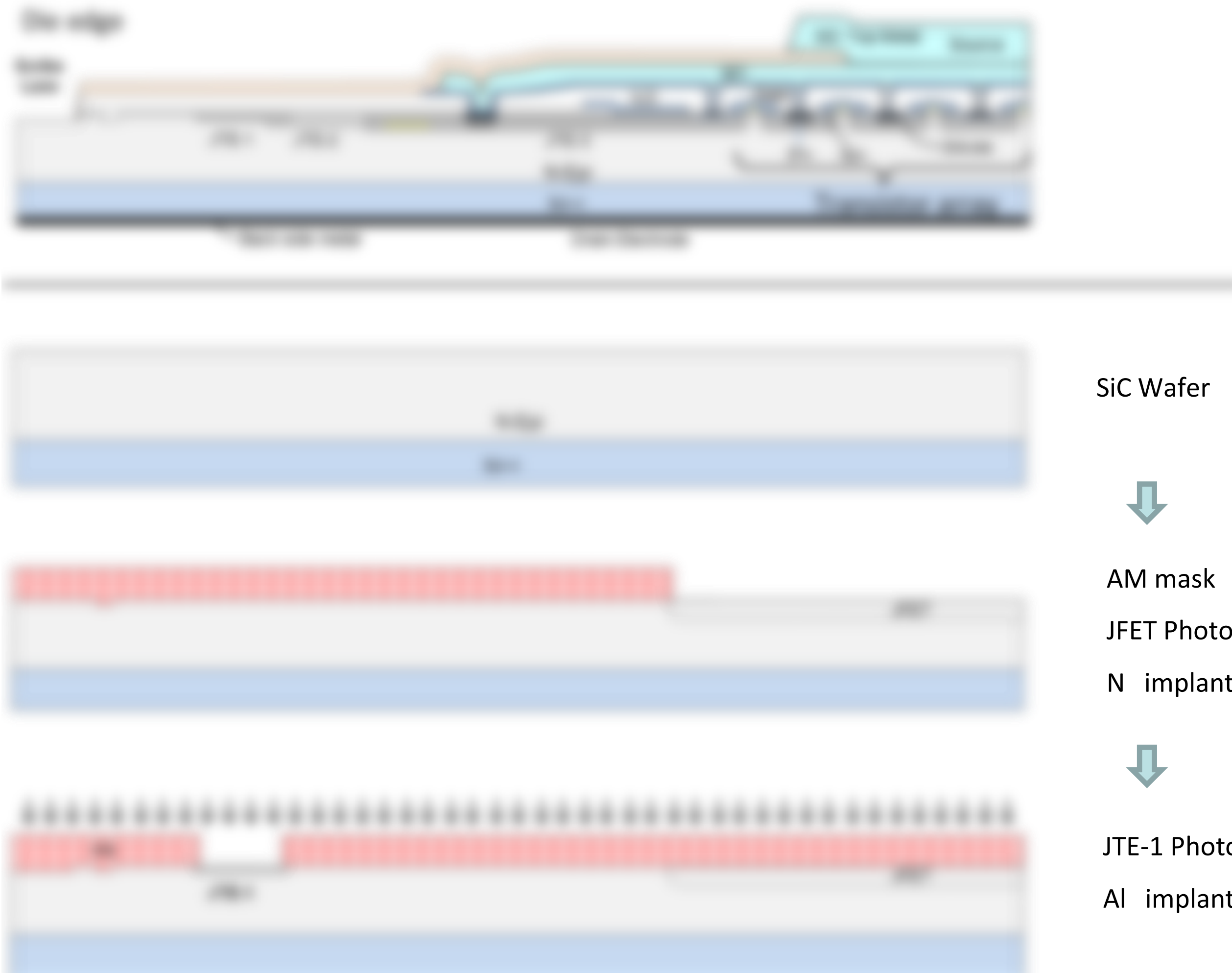
Mask	Process	Comment
[9]	GP (Gate Poly) Photomask	[illegible]
	PolySi etch	
	PECVD oxide deposition	[illegible]
[10]	SO (Silicide) Photo	[illegible]
	PECVD etching	[illegible]
	Silicide metal Sputter	[illegible]
	Silicidation	[illegible]
	ILD1 (B)PSG deposition	[illegible]
	Reflow melting	[illegible]
[11]	CO (Contact) Photo	[illegible]
	CO ILD etching	[illegible]
	Al Metal depostion	[illegible]
[12]	M1 (Metal) Photo	
	Metal etching	[illegible]
	ILD2a CVD oxide deposition	[illegible]
[13]	VHA Photo	
	ILD2a etching	
	ILD2b CVD oxide deposition	[illegible]
[14]	VHB Photo	
	ILD2b etching	
	ILD2c CVD oxide deposition	[illegible]
[15]	VIA Photo	
	ILD etching	
	Al-2 Metal deposition	[illegible]
[16]	M2 (Metal) Photo	
	Metal etching	
	Passivation layer deposition	[illegible]
[17]	BW (Bonding Window) Photo	
	Passivation layer etching	
	Wafer backside grinding	[illegible]
	Backside metal deposition	[illegible]
	Dicing (singulation)	

・It is estimated that 17 photo/masking steps are used for the front-end process up to the backside metallization process.

4-2. SiC MOSFET process sequence cross sections

Cross-sectional view and layout top view of onsemi's NTH4L022N120M3S SiC MOSFET

Process sequence of onsemi NTH4L022N120M3S SiC MOSFET (estimated) (1)



SiC Wafer

AM mask
JFET Photo
N implant

JTE-1 Photo
Al implant

5. Device structure and electrical characteristics analysis

In this section the measurement results of the following electrical characteristics are analyzed.

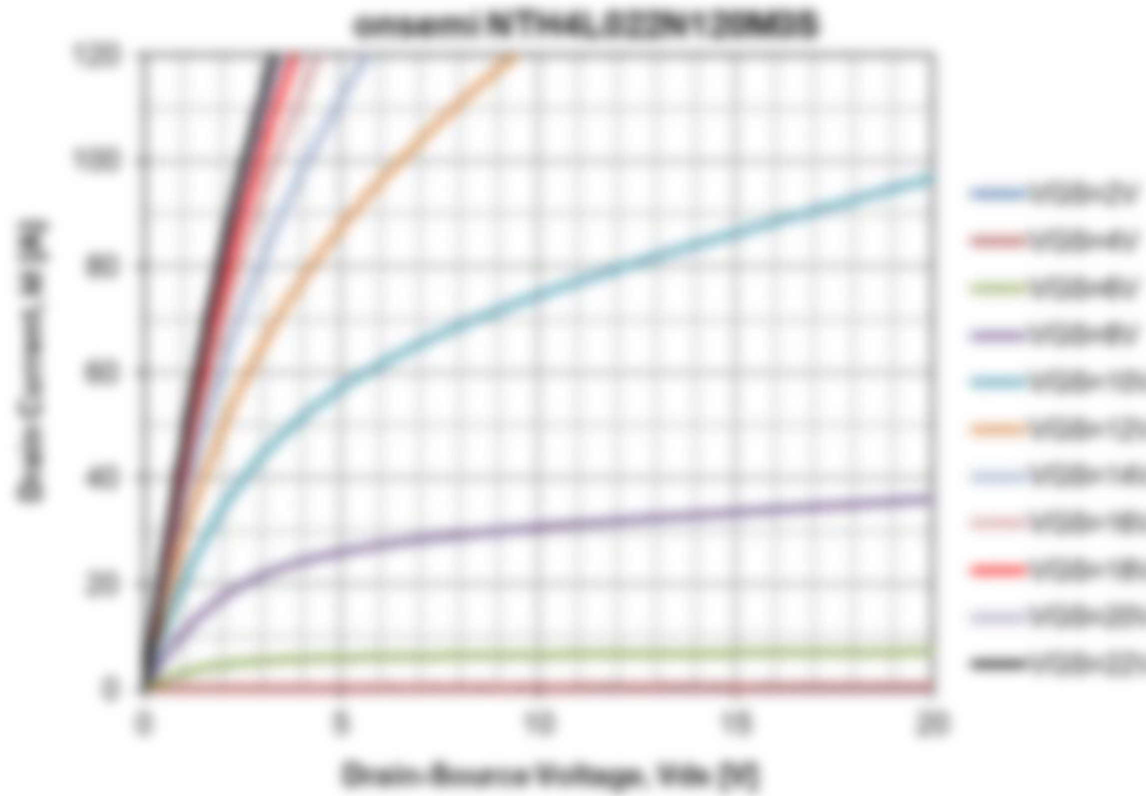
1. Id-Vds characteristics
2. Off-State drain current Idss vs. drain voltage (Vds) with device temperature as parameter, and activation energy (Ea)
3. Off-state breakdown voltage BVdss characteristics and operation margin
4. Leakage current comparison between SiC MOSFETs manufacturers
5. Body diode characteristics
6. Capacitances (Ciss, Coss, Crss)-Vds characteristics

Furthermore, the correlation between the electrical characteristics and the physical structure of the transistor is considered,

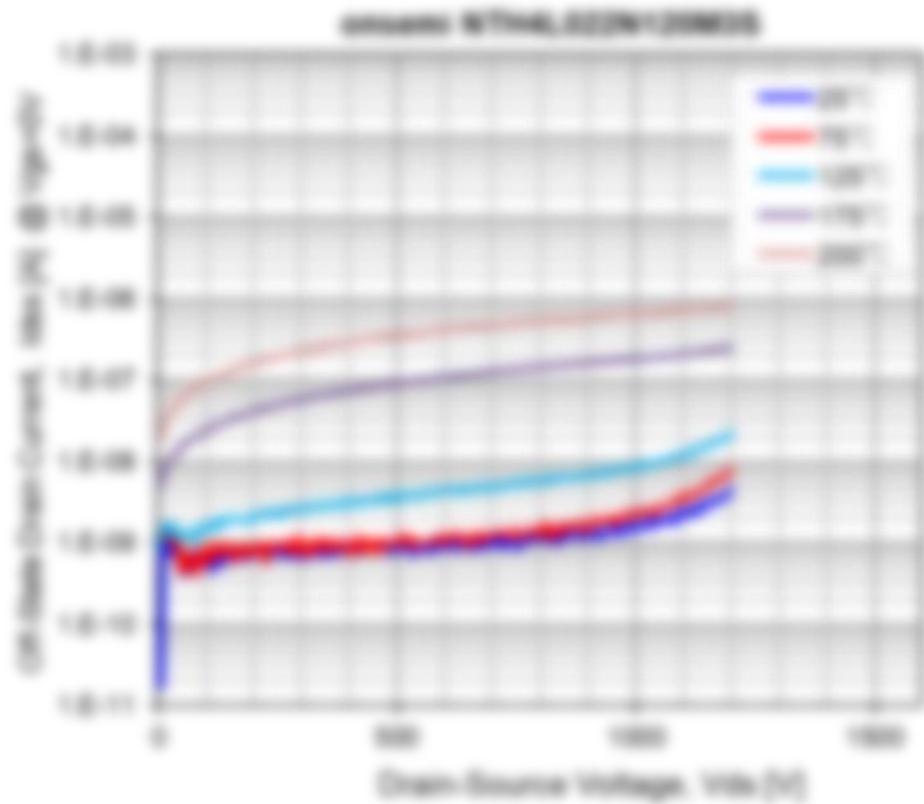
7. Device structure and electrical characteristics analysis: ON resistance
8. N-Epi layer impurity concentration analysis

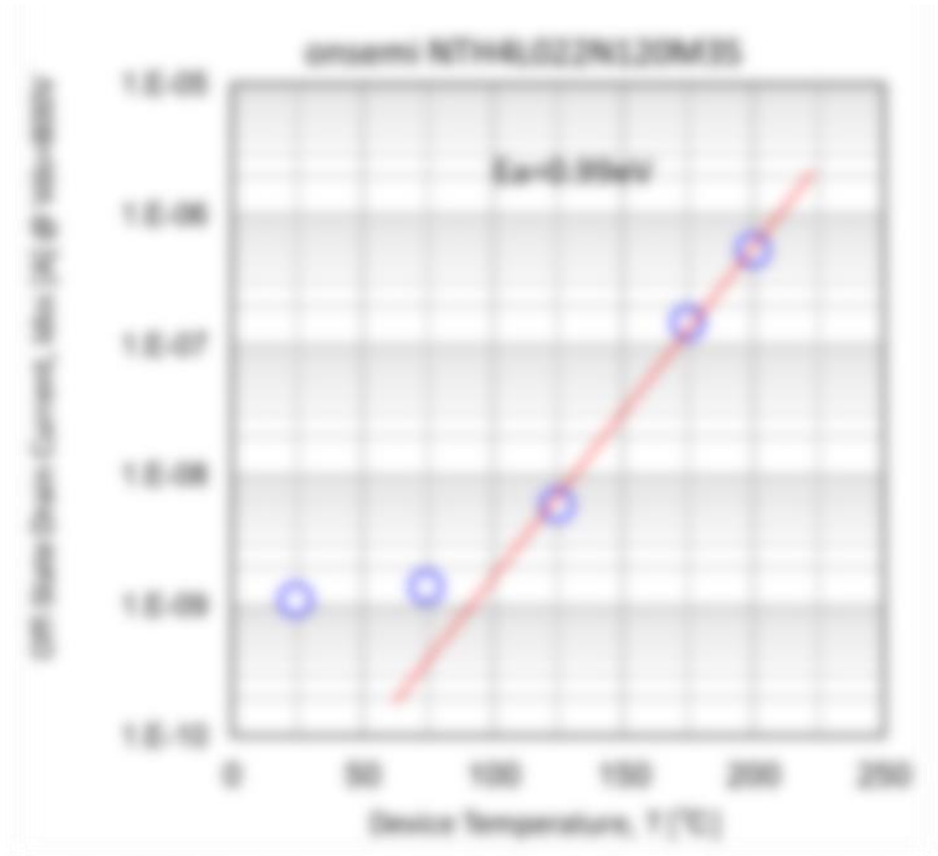
The data presented in this section do not represent a wide range of statistical samples but can still be considered as reference values. In addition, it is worth noting that systematic and regular evaluations should be considered as manufacturers are constantly striving to improve the manufacturing process for SiC wafers and epilayers.

5-1. SiC MOSFET NTH4L022N120M3S Id-Vds characteritics



5-2. Off-State drain current Idss vs. drain voltage (Vds) and activation energy (Ea)

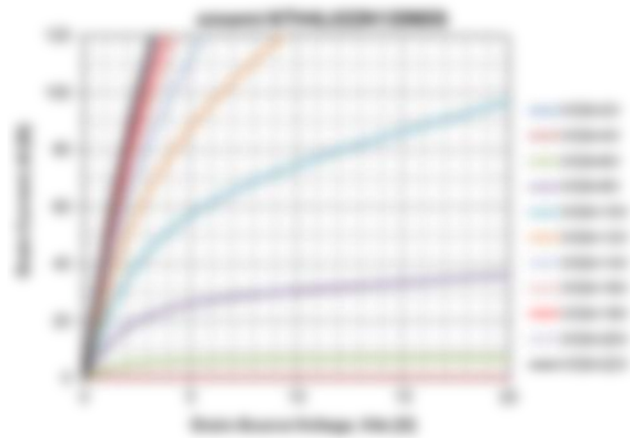


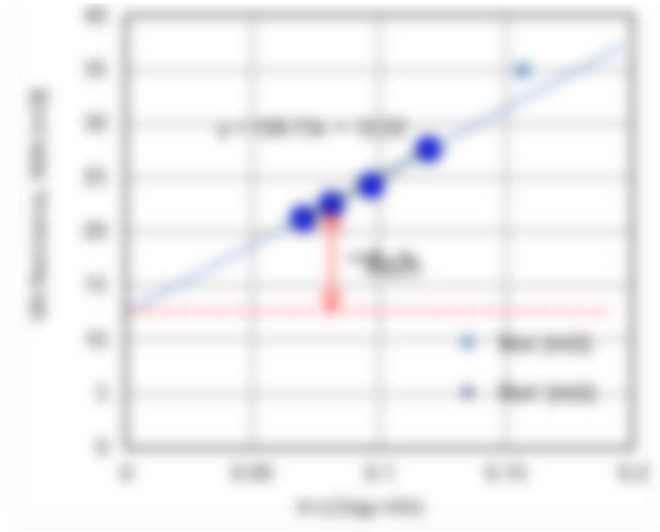


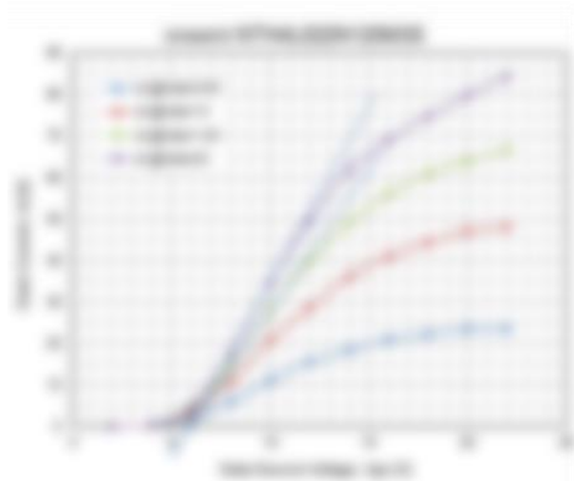
The on-resistance components are estimated by analysis of the measured Id-Vds-Vgs characteristics and device structure data.

1) Rch accounts for about 45% of Ron.

2) The thick SiC substrate resistance, Rsub accounts for about 8% of Ron.







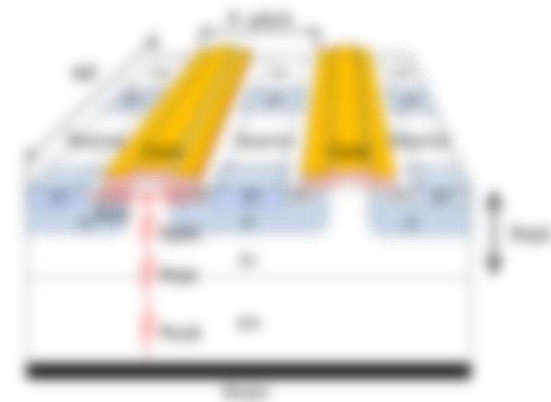


Fig. 5-7-1 SiC MOSFET Characteristics for RON Analysis

6. Related references

7. Related patents

United States Patent

(57) ABSTRACT

In one general aspect, an apparatus can include a semiconductor region including a silicon carbide material and a junction termination extension implant region disposed in the semiconductor region. The apparatus can include a low interface state density portion of a dielectric layer having at least a portion in contact with the junction termination extension implant region.

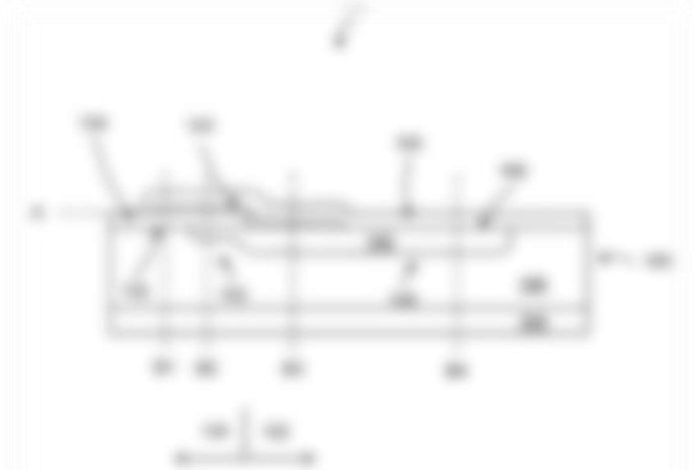


FIG. 1

FIG. 2

Junction Termination Extension (JTE) related patent