Mar 23, 2023

Product Analysis Report

No. 22G-0037-1 Onsemi Structure Analysis

Product : SiC MOSFET

Part No. : NTH4L022N120M3S

Manufacturer : ON Semiconductor Corporation

Package : TO-247-4

Marking : H4L022
120M3S
ON 1N35AA

Die size : SiC MOSFET

Process : SiC wafer, Planar gate, upper source : 2-layer metal process

Report content: Structural analysis and SCM analysis

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1. Device Summary

Table1-1： Device summary

Product type	[illegible]
Manufacturer	[illegible]
Part number	[illegible]
Package	[illegible]
Package marking	[illegible]
Die configuration	[illegible]
SiC-MOSFET Die size	[illegible]
SiC-MOSFET Chip manufacturing process	[illegible]
SiC-MOSFET Metal interconnect	[illegible]
Characteristic Feature	[illegible]
Applications	[illegible]

1-1. Summary of analysis results

Package appearance

Cross-sectional structure analysis

SiC-MOSFET Die

Die size : [redacted] mm²

・planar-type gate, upper source metal 2-layer metal process
・ The die edge withstand voltage structure uses a three-step JTE (Junction Termination Extension)

Die outer periphery

Source electrode

Table1-3: Device structure： Layers material and thickness

Layer description	[illegible]	[illegible]	[illegible]
Wafer type・configuration (Bulk, Epi)	[illegible]	[illegible]	[illegible]
N-epi layer	[illegible]	[illegible]	[illegible]
N Buffer layer	[illegible]	[illegible]	[illegible]
Pwell implant depth	[illegible]	[illegible]	[illegible]
N+ implant depth	[illegible]	[illegible]	[illegible]
Gate electrode structure/material	[illegible]	[illegible]	[illegible]
Gate dielectric layer	[illegible]	[illegible]	[illegible]
Field oxide layer	[illegible]	[illegible]	[illegible]
Silicide layer	[illegible]	[illegible]	[illegible]
Source barrier layer (M1)	[illegible]	[illegible]	[illegible]
Source metal M1	[illegible]	[illegible]	[illegible]
Source barrier layer (M2)	[illegible]	[illegible]	[illegible]
Source metal M2	[illegible]	[illegible]	[illegible]
ILD1 (Between gate and M1)	[illegible]	[illegible]	[illegible]
ILD2 (Between M1-M2)	[illegible]	[illegible]	[illegible]
Protection layer	[illegible]		
Die back-side metal	[illegible]	[illegible]	[illegible]

2. Package Analysis

2-1. Appearance observation

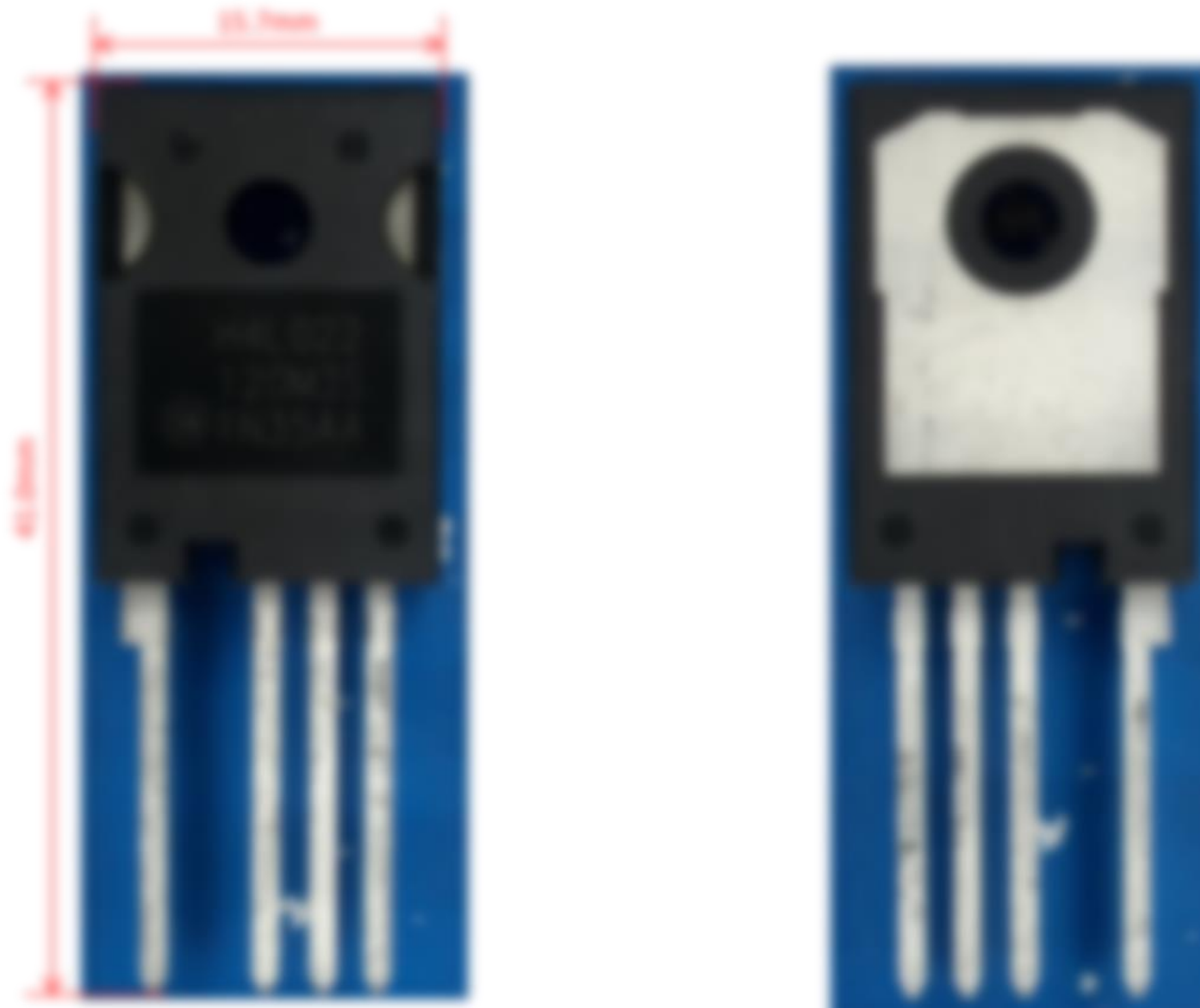


Fig. 2-1-1 Package observation

2-1. Appearance observation

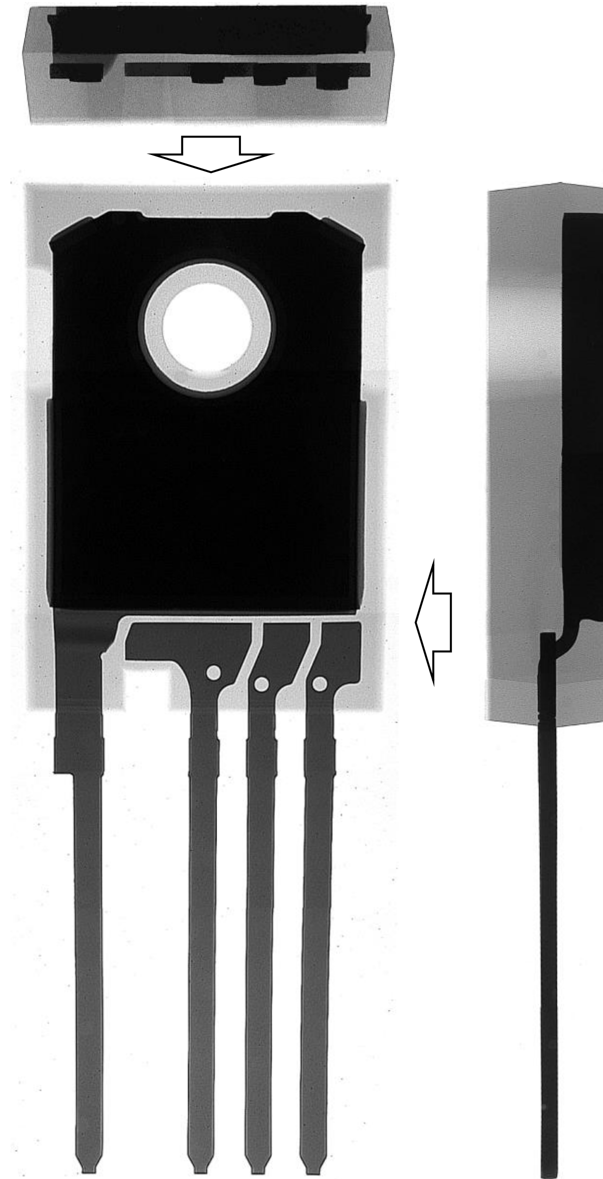


Fig. 2-1-2 X-ray image (front/side)

2-1. Appearance observation

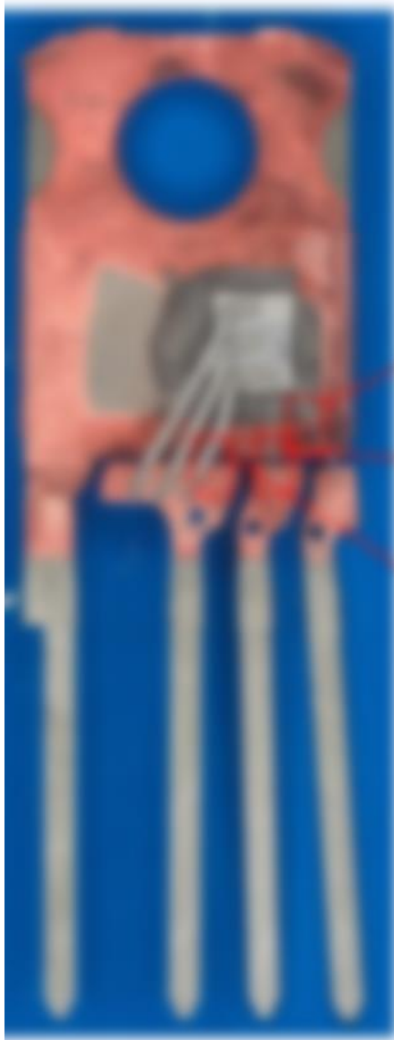
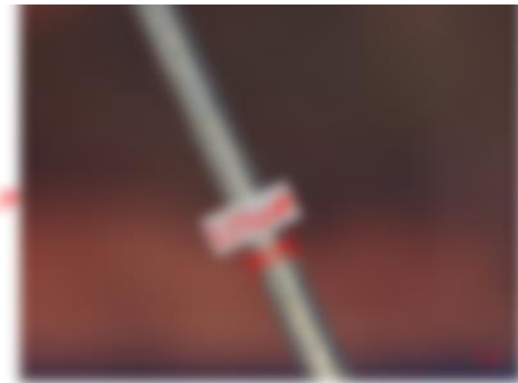


Fig. 2-1-3 Internal layout observation



2-2. Die Observation

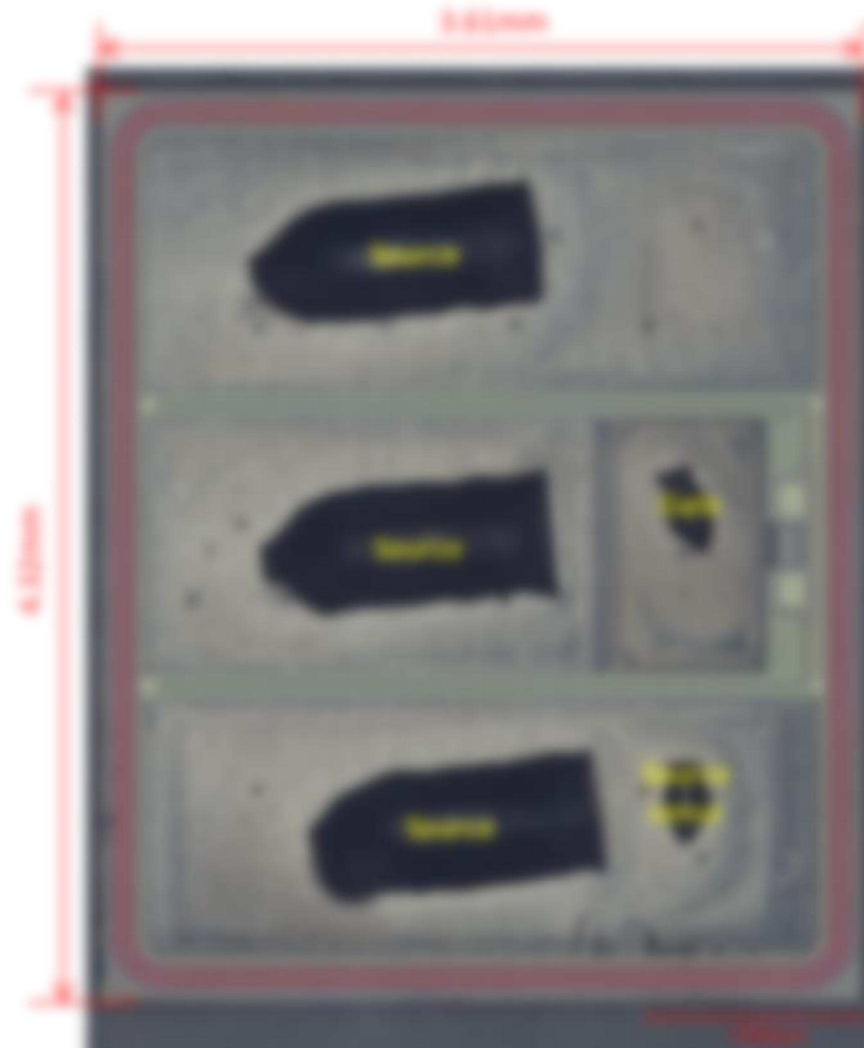


Fig. 2-2-1 Die picture (Top Metal layer)

3. SiC MOSFET structure analysis

3-1. Plane structure analysis by Optical Microscope

Die size
Active area

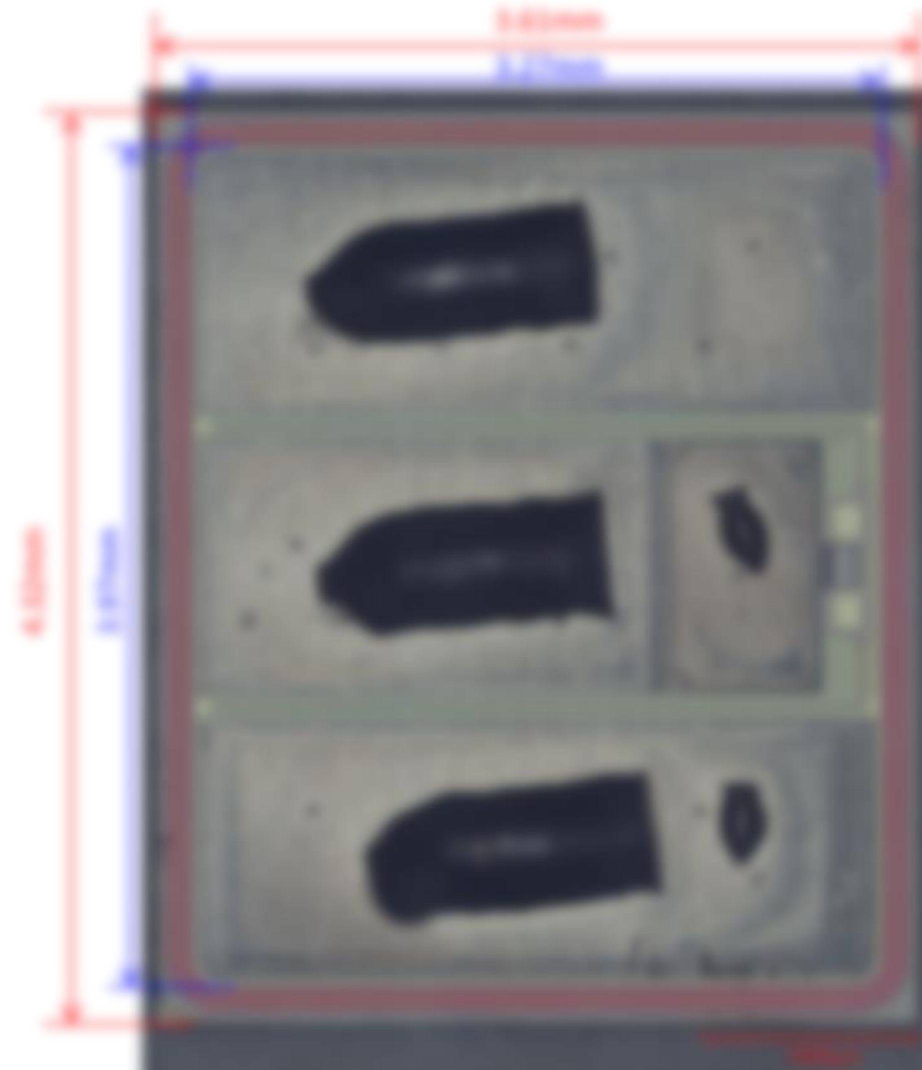


Fig. 3-1-1 Die photo (Top Metal layer)

3-1. Plane structure analysis by Optical Microscope

※In this chip layout the gate resistor is shorted by M1.

【Top Metal】

Fig. 3-1-4 Gate electrode pad (Top Metal layer)

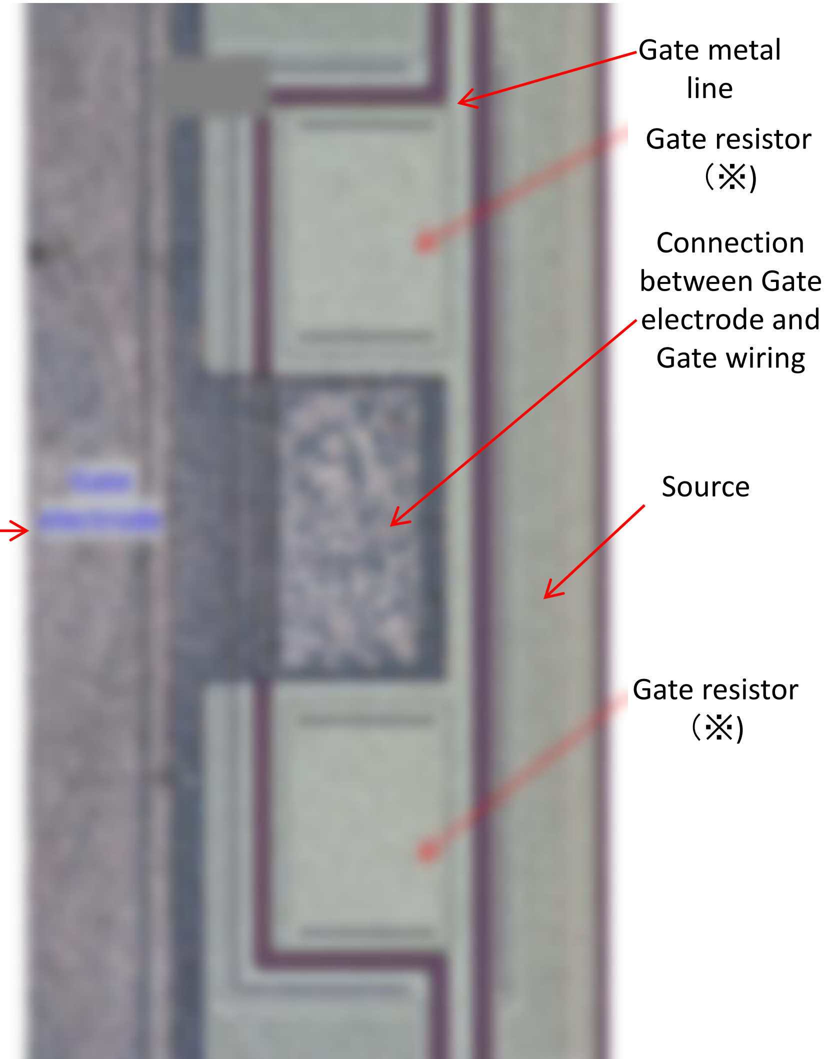


Fig. 3-1-5 Gate electrode pad (Top Metal layer)

3-1. Plane structure analysis by Optical Microscope

【Poly-Si layer (Top Metal removed)】

Cell array

Fig. 3-1-17 Gate Pad area (Poly-Si layer)

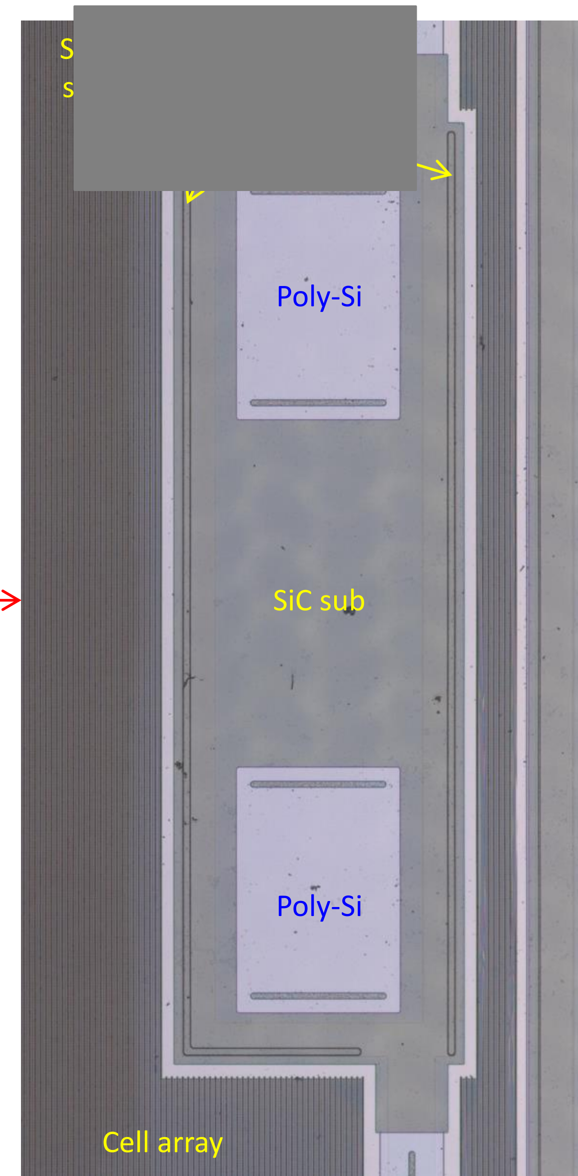


Fig. 3-1-18 Gate Pad Gate resistor (Poly-Si layer)

3-2. Plane structure analysis by SEM

【Poly-Si layer (Top Metal removed)】

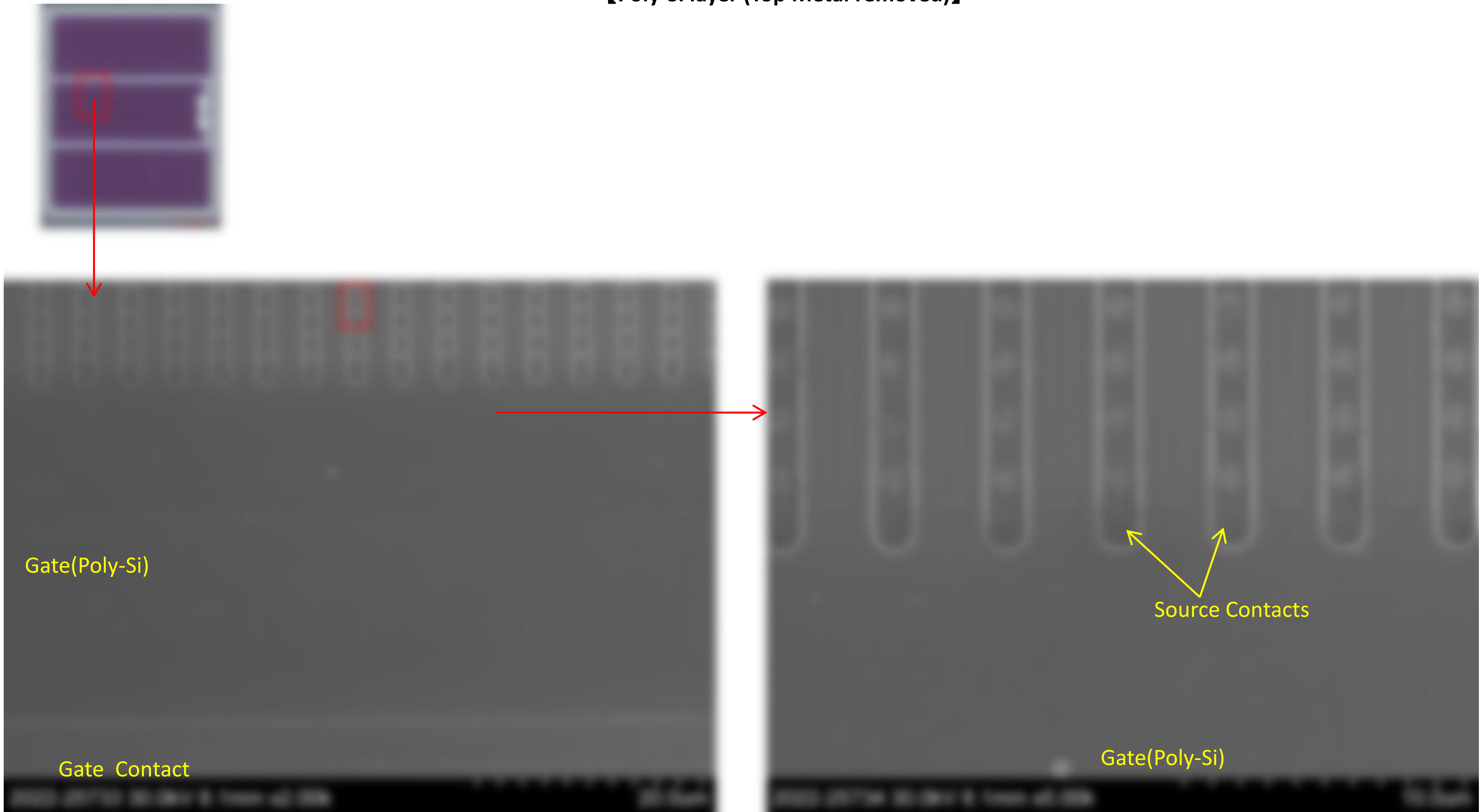
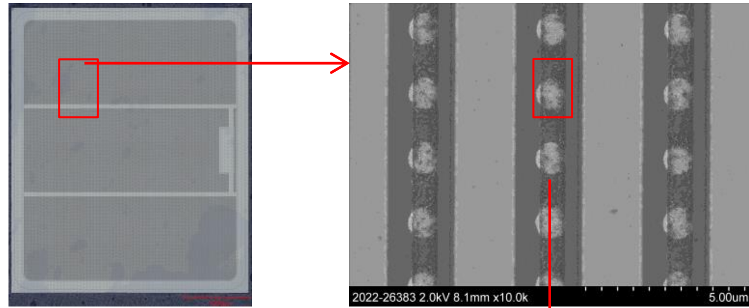


Fig. 3-2-5 Cell area edge plane SEM image (Poly-Si layer)

Fig. 3-2-6 Cell area edge plane SEM image (Poly-Si layer)

3-2. Plane structure analysis by SEM

【SiC substrate layer (Poly-Si, isolation films removed)】



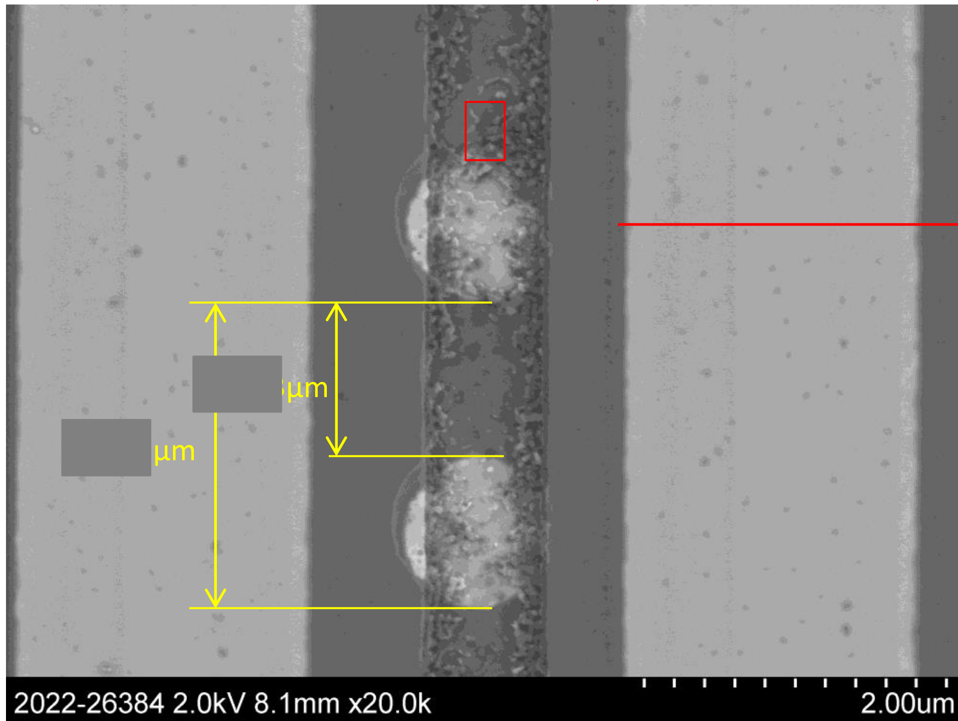


Fig. 3-2-18 Cell area plane SEM image (SiC substrate layer)

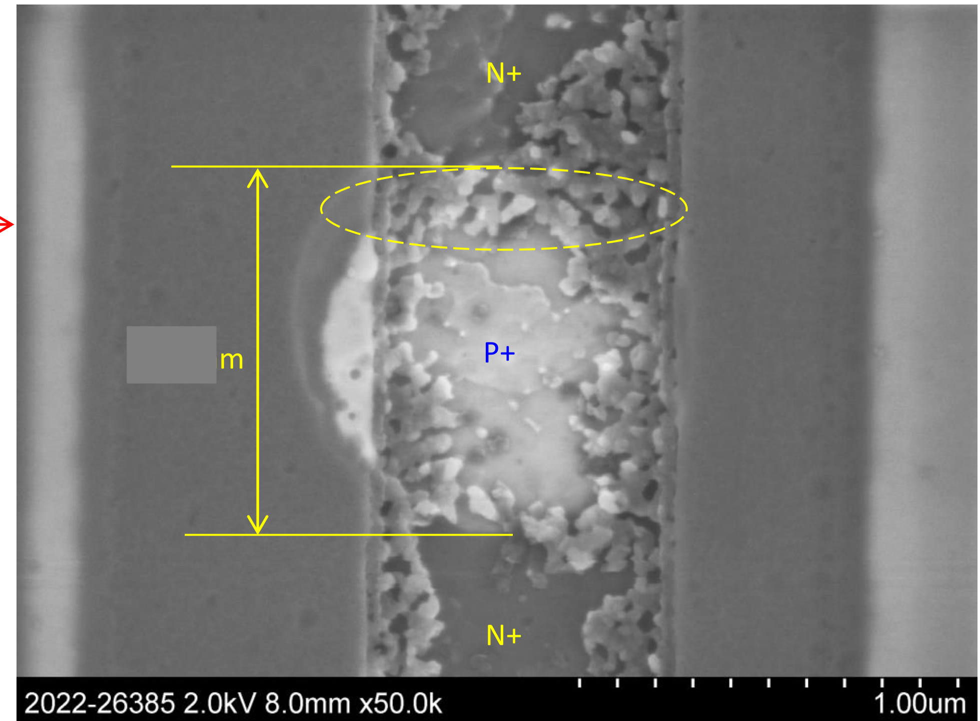


Fig. 3-2-19 Cell area plane SEM image (SiC substrate layer)

3-3. Cell area cross-sectional structure analysis

Fig. 3-3-1 Die image (Top Metal layer)

3-3. Cell area cross-sectional structure analysis

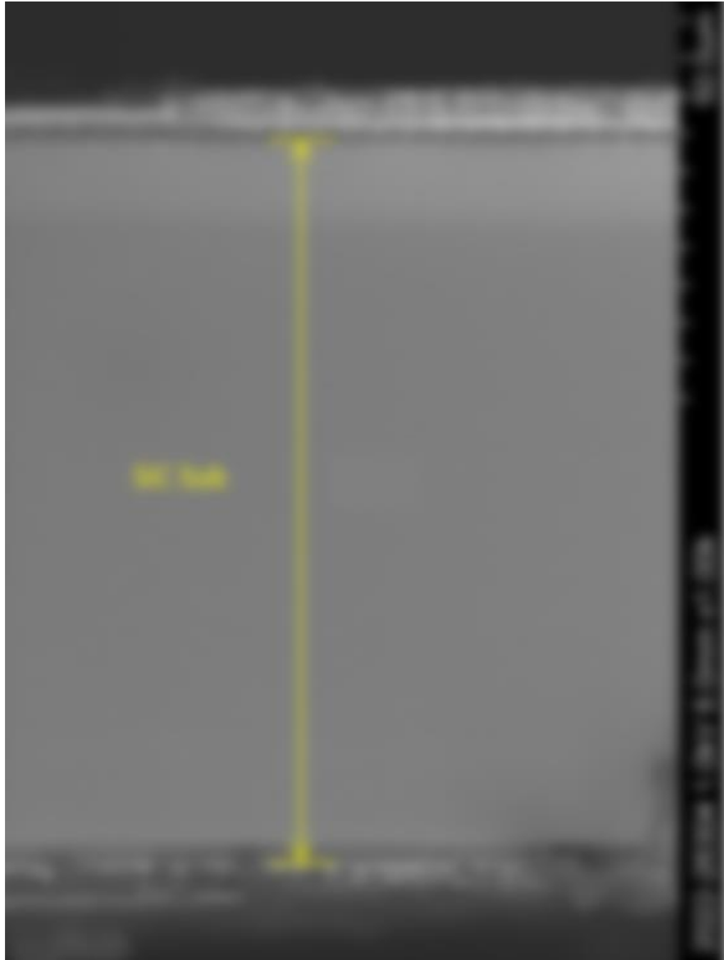


Fig. 3-3-2 Die cross-section SEM image

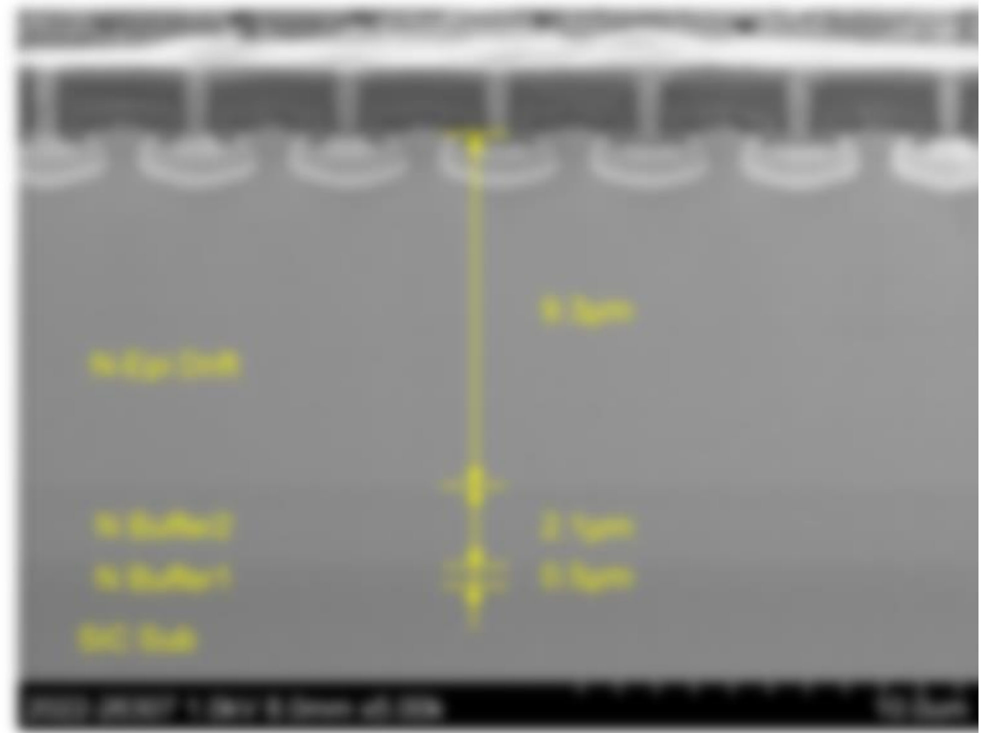


Fig. 3-3-3 N-Epi layer SEM image

3-3. Cell area cross-sectional structure analysis

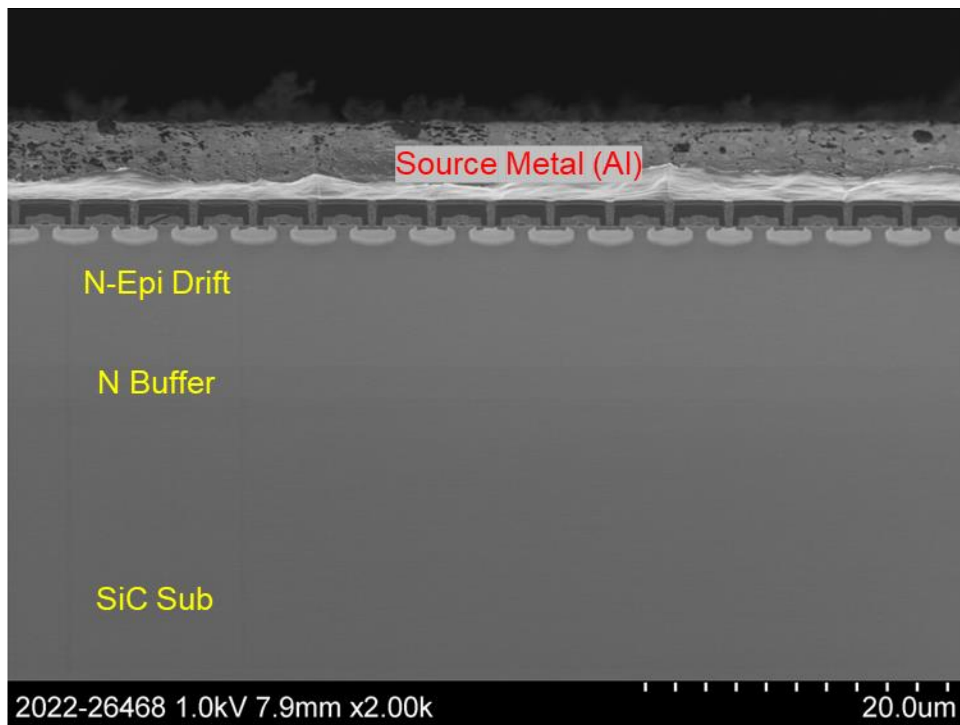


Fig. 3-3-4 Cell area cross-sectional SEM image

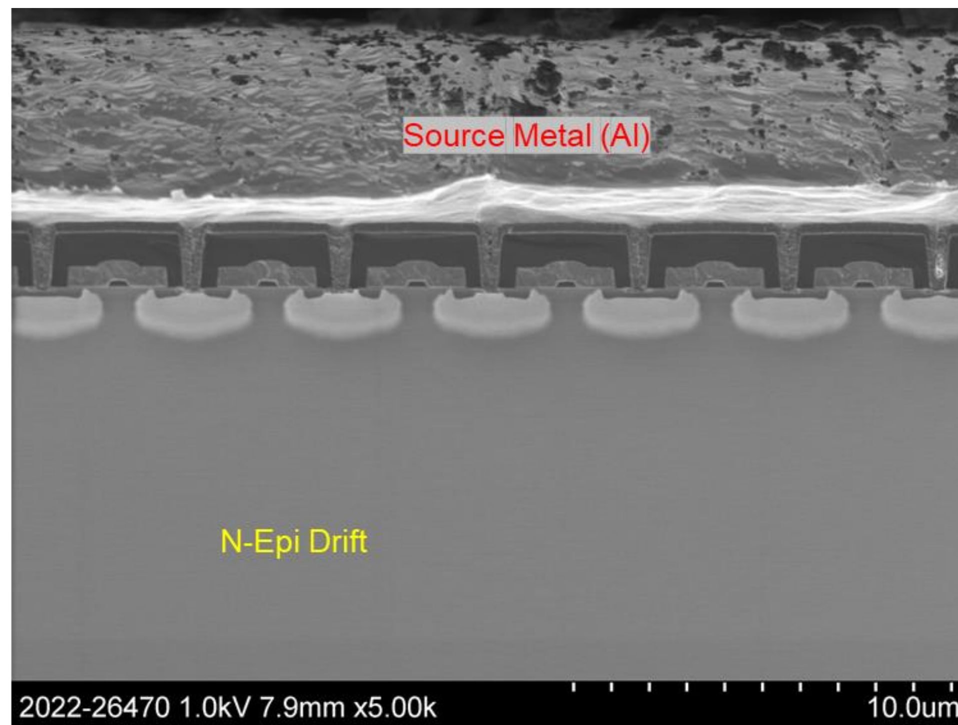


Fig. 3-3-5 Cell area cross-sectional SEM image

※Implanted layer estimate

3-3. Cell area cross-sectional structure analysis

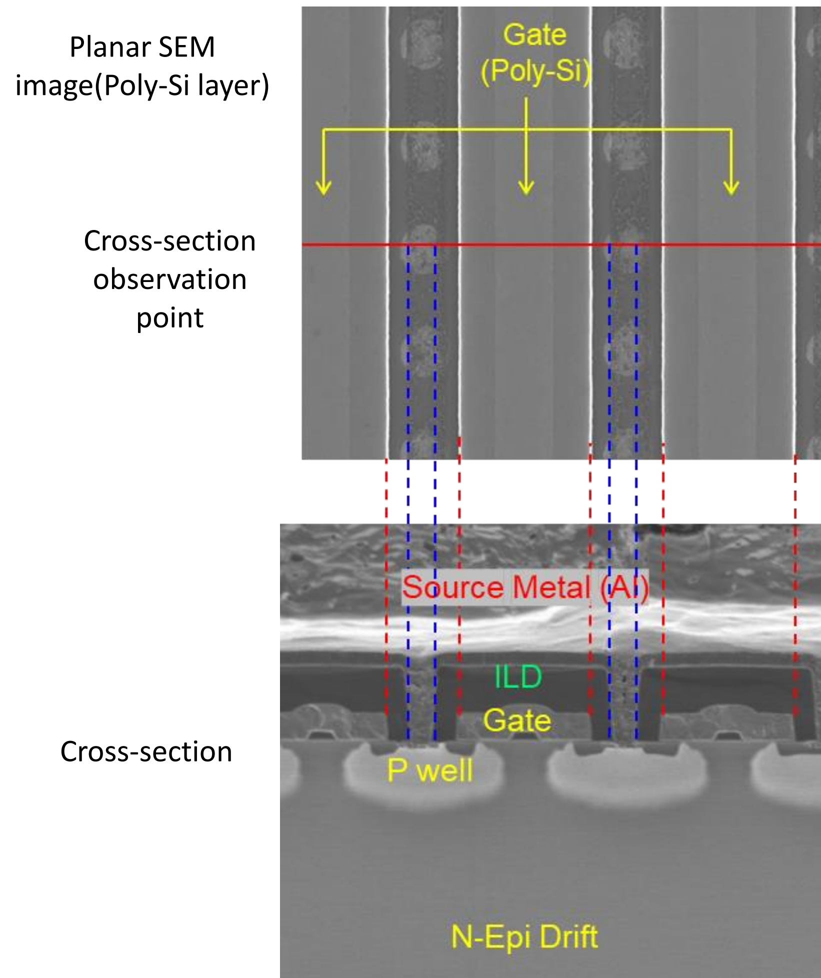


Fig. 3-3-6 Cell area SEM image

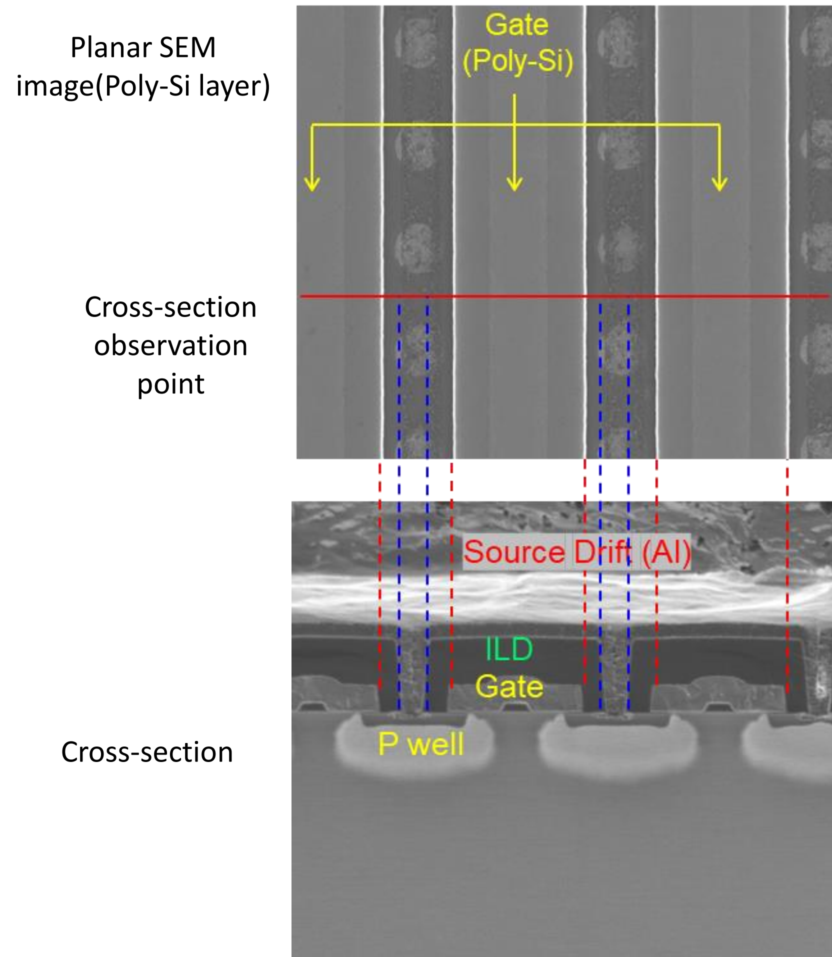


Fig. 3-3-7 Cell area SEM image

3-3. Cell area cross-sectional structure analysis

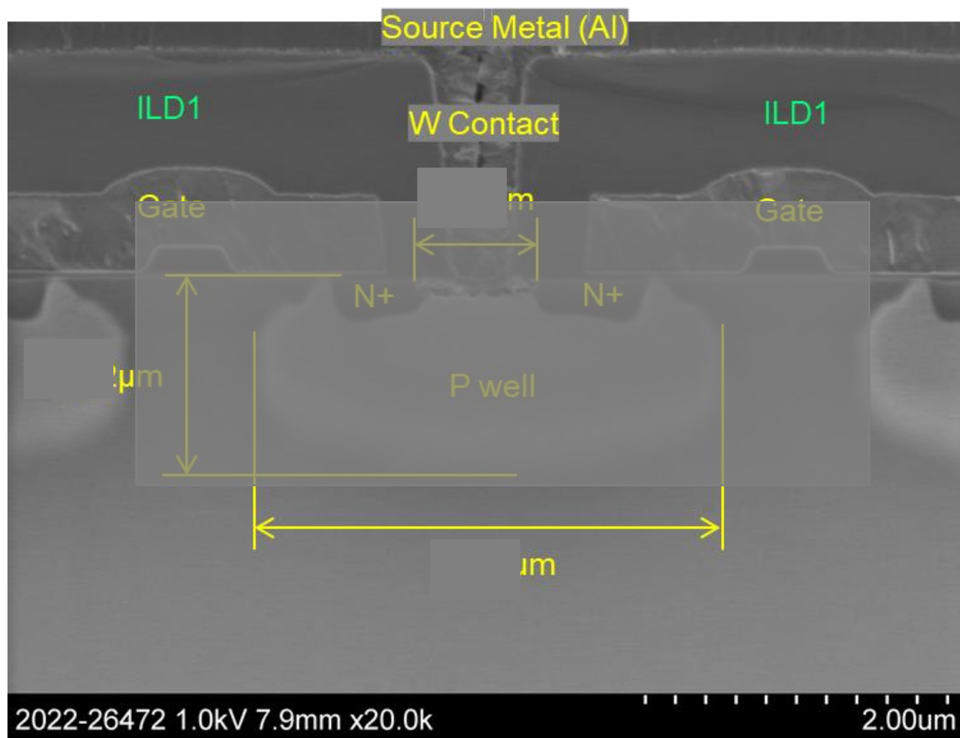


Fig. 3-3-10 Cell area SEM image

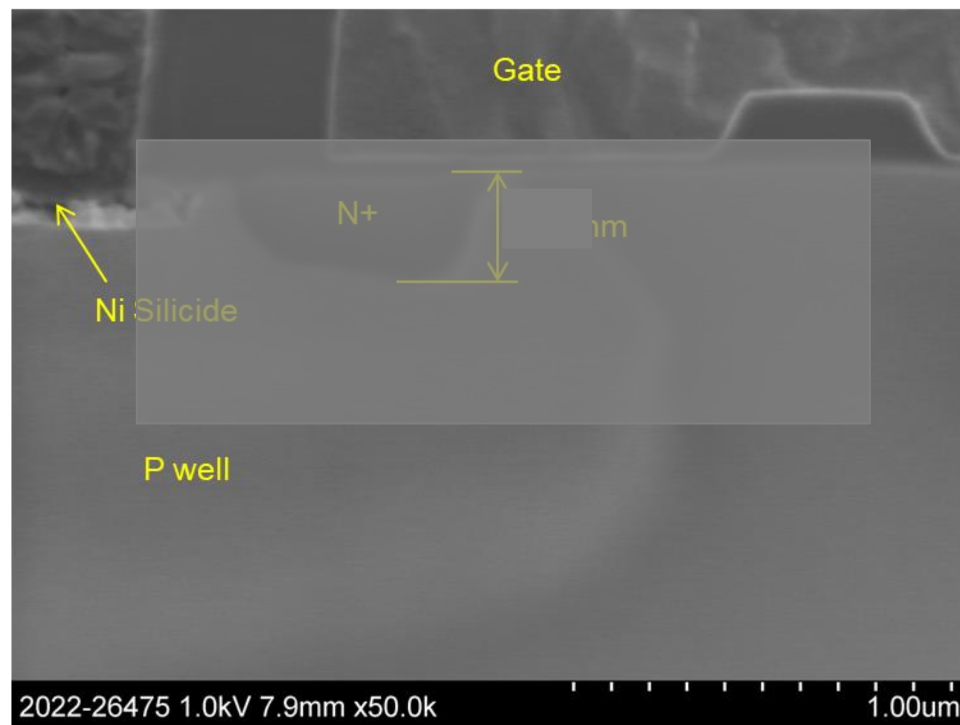


Fig. 3-3-11 Cell area SEM image

3-3. Cell area cross-sectional structure analysis

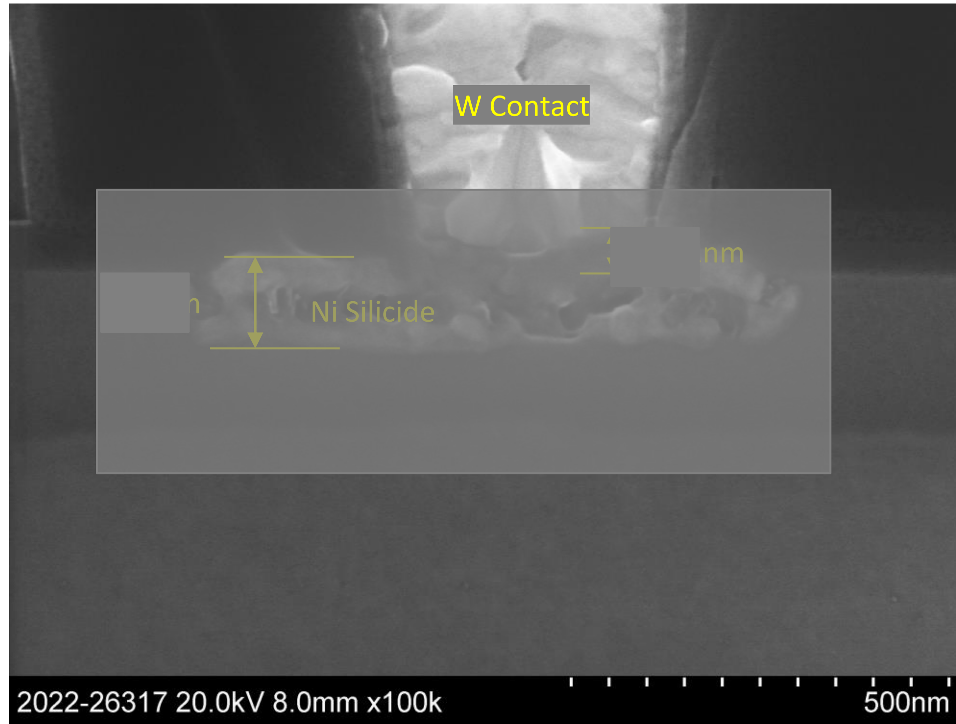


Fig. 3-3-17 Cell area SEM image

3-5. MOSFET gate pad cross-sectional structure analysis

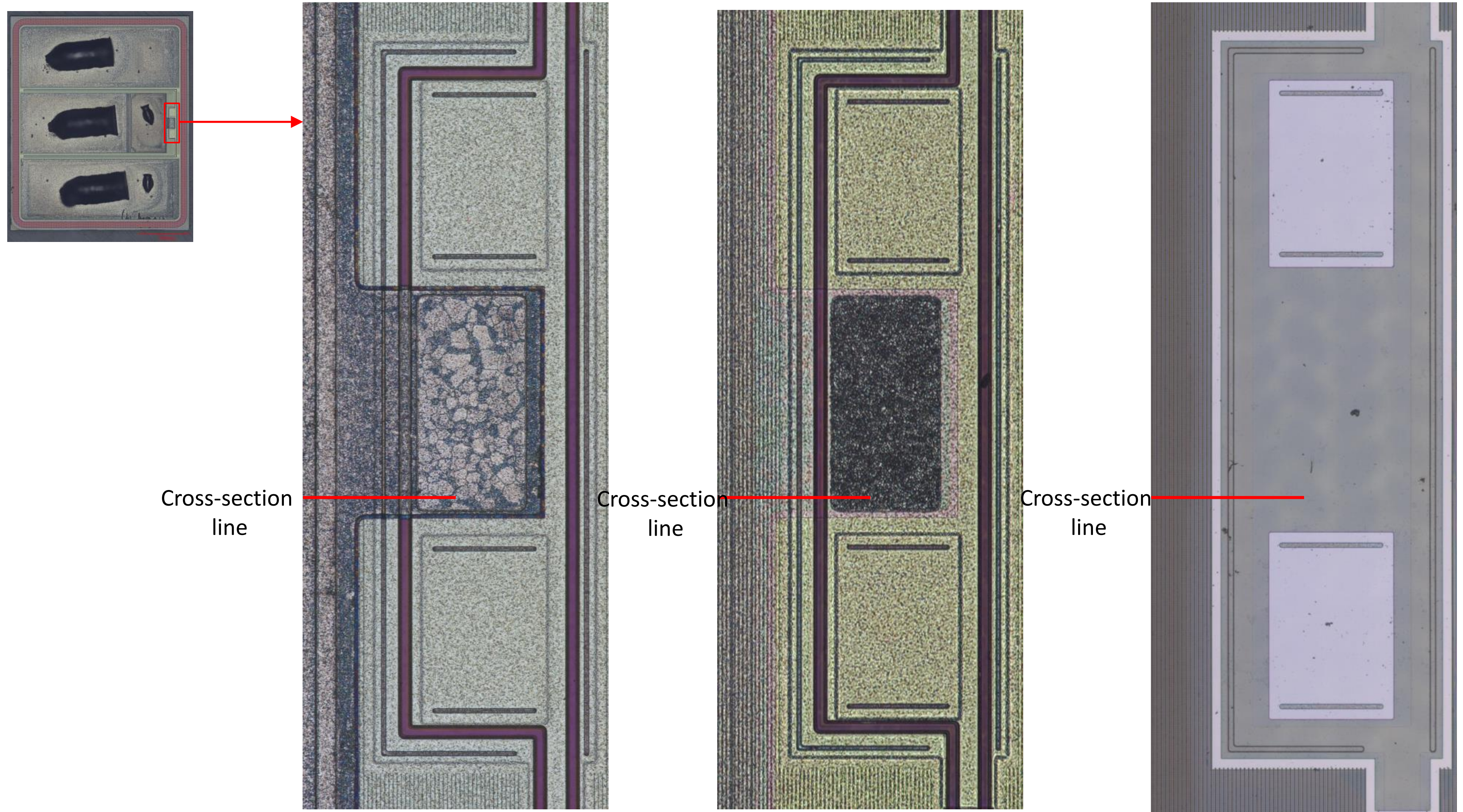
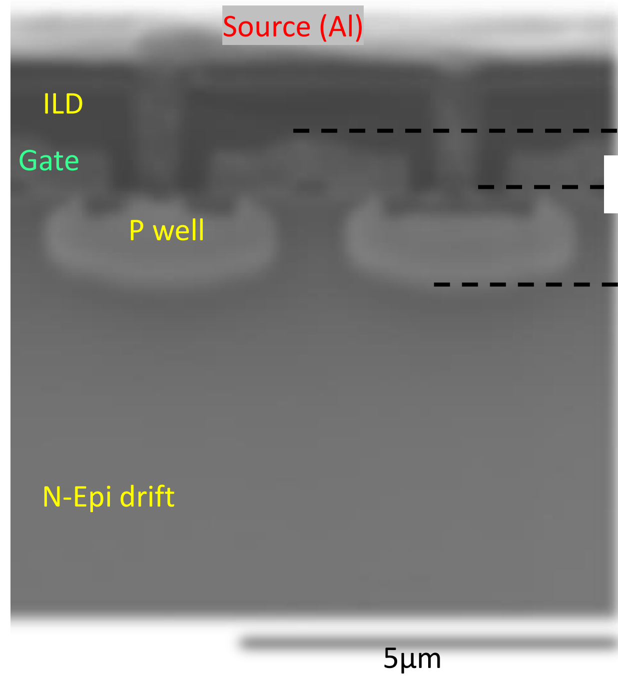


Fig. 3-5-1 Gate Pad cross-section processing location

4. SCM / SMM Analysis

4-1. SCM / SMM Analysis Results



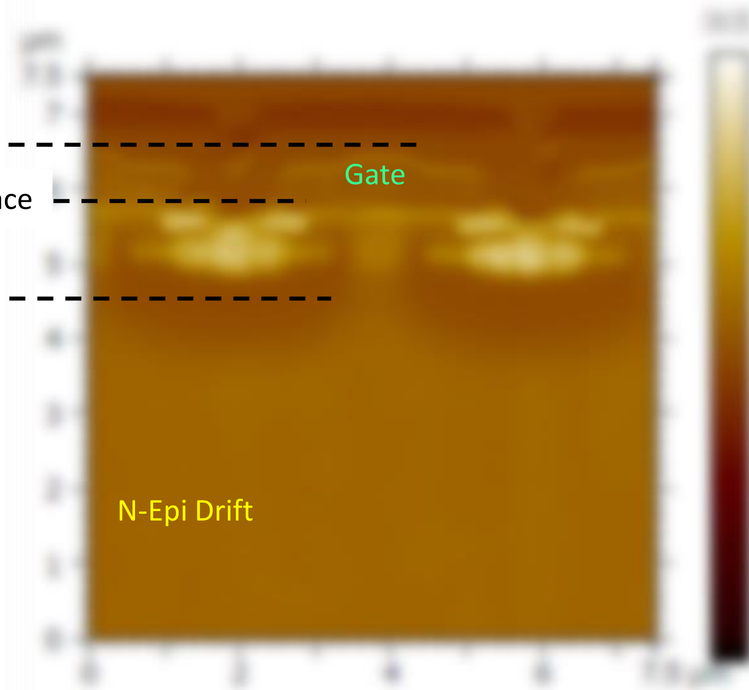


Fig. 4-1-1 Cell area cross-sectional SEM.

Fig. 4-1-2 Cell area cross-sectional AFM.

4-1. SCM / SMM Analysis Results

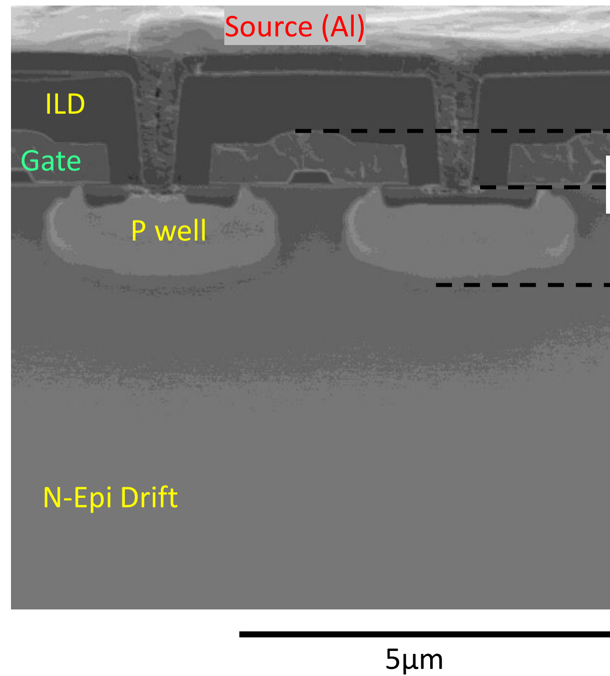


Fig. 4-1-5 Cell area cross-sectional SEM.

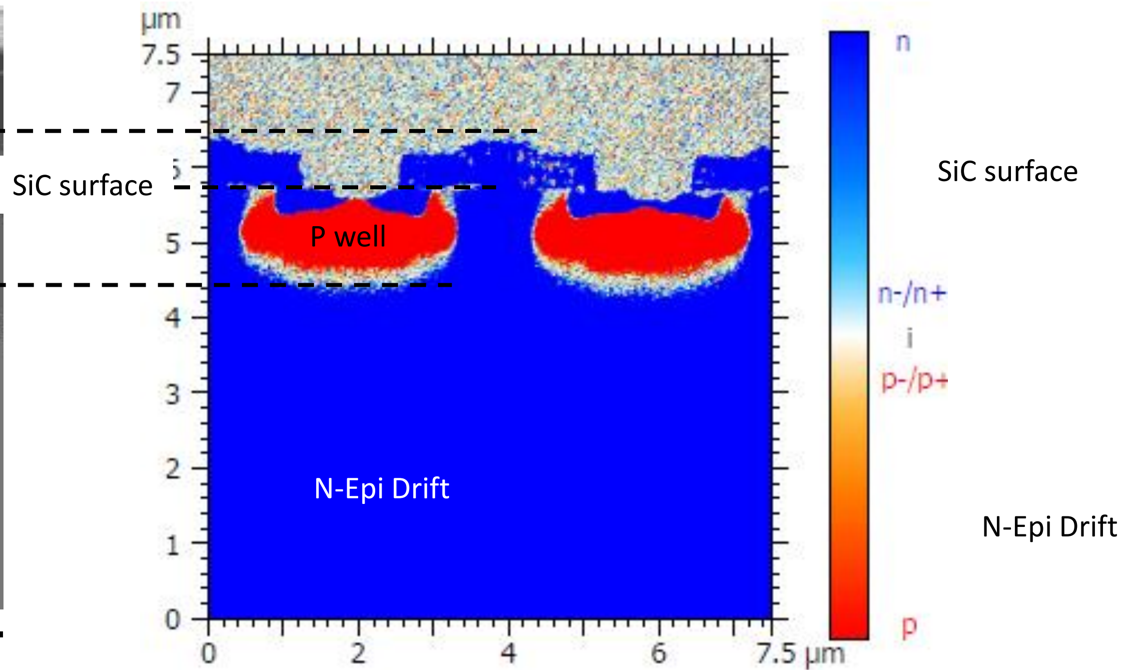


Fig. 4-1-6 Cell area SCM image (scale enhancement)

4-1. SCM / SMM Analysis Results

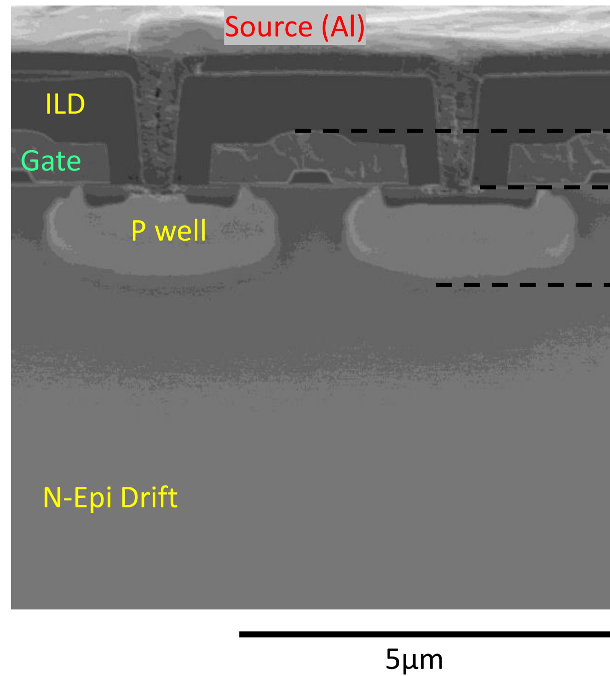


Fig. 4-1-7 Cell area cross-sectional SEM.

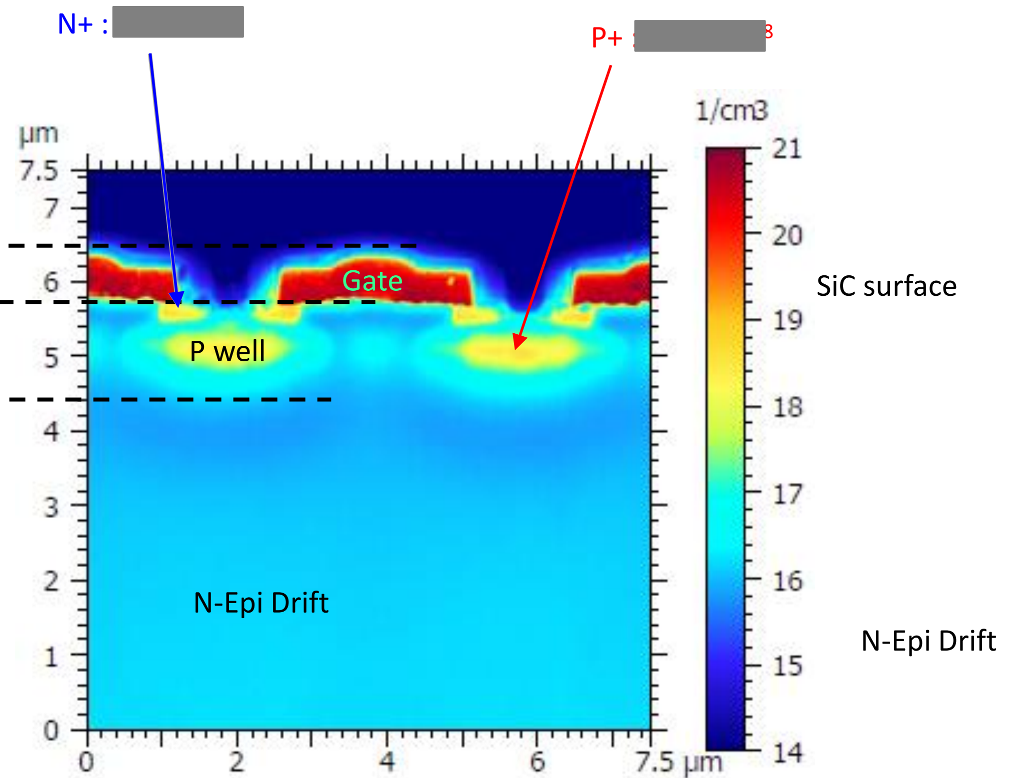


Fig. 4-1-8 Cell area SMM carrier concentration conversion image

4-2. SCM / SMM Line Analysis

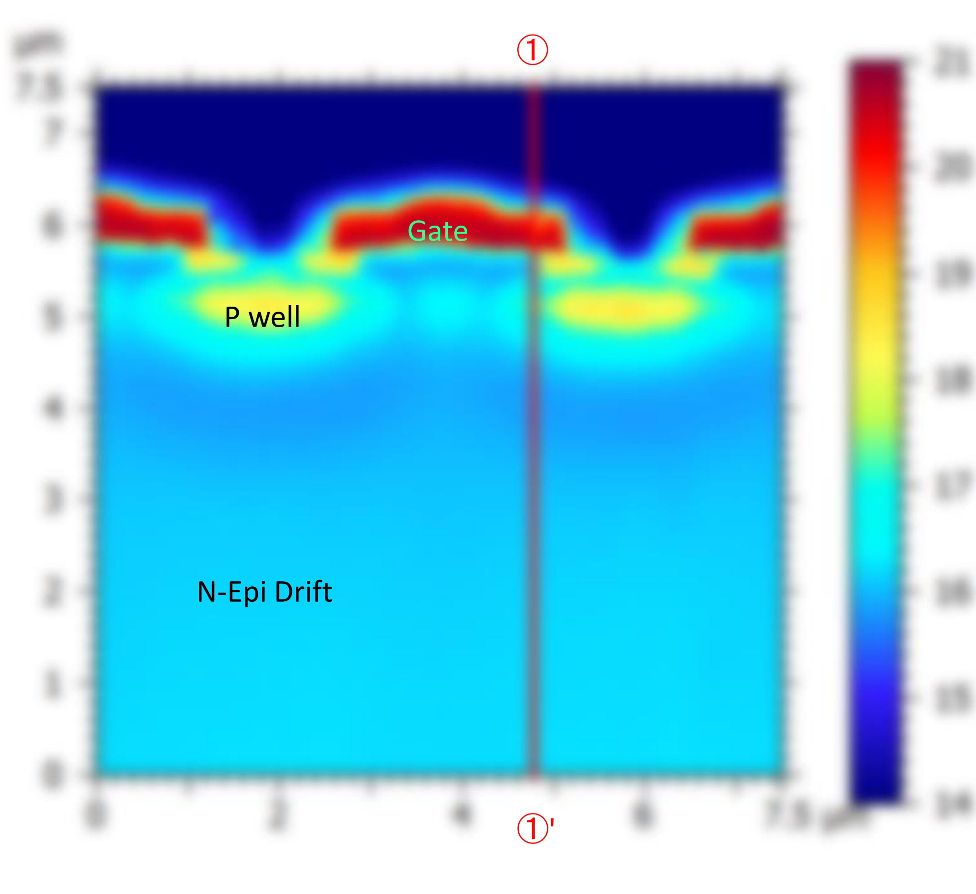


Fig. 4-2-1 Cell area SMM carrier concentration conversion image

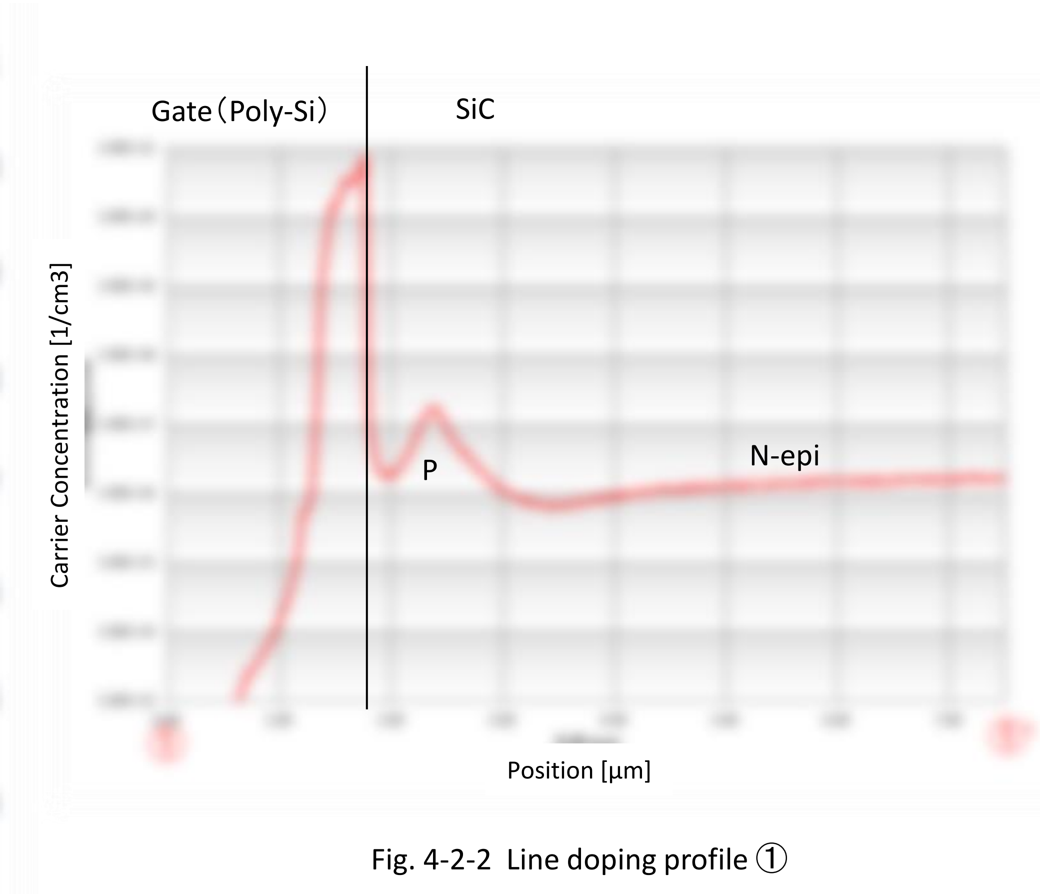


Fig. 4-2-2 Line doping profile ①