

Product Analysis Report

No. 22G-0037-1	Onsemi Structure Analysis
Product	: SiC MOSFET
Part No.	: NTH4L022N120M3S
Manufacturer	: ON Semiconductor Corporation
Package	: TO-247-4
Marking	: H4L022 120M3S ON 1N35AA
Die size	: SiC MOSFET <small>(Width: 4.0mm x 15.0mm)</small>
Process	: SiC wafer, Planar gate, upper source : 2-layer metal process
Report content:	Structural analysis and SCM analysis

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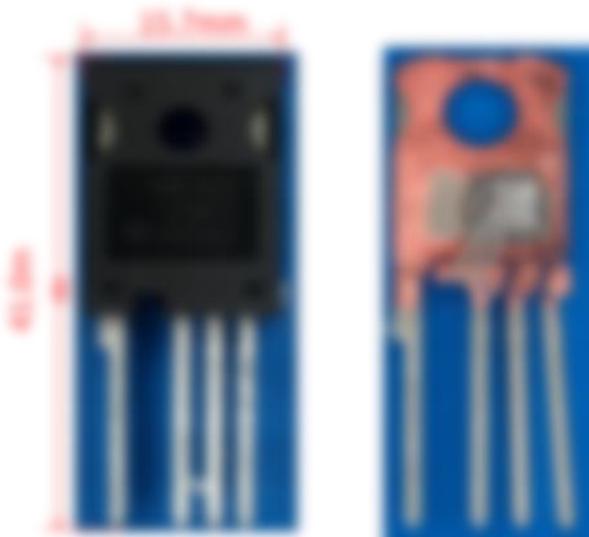
1. Device Summary

Table1-1: Device summary

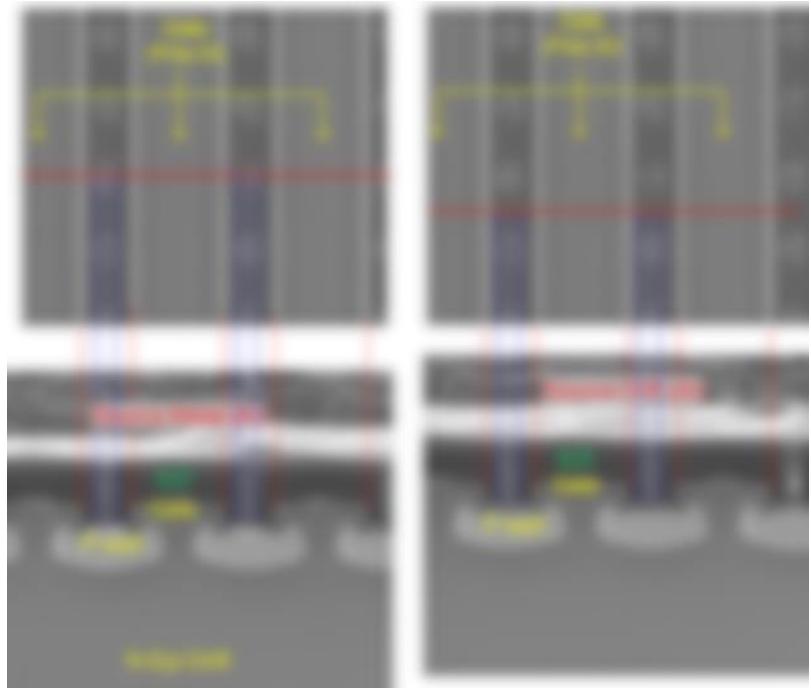
Product type	SiC MOSFET
Manufacturer	ON Semiconductor
Part number	NTH4L022N120M3S
Package	TO-220AB
Package marking	00000000000000000000000000000000
Die configuration	Single die
SiC-MOSFET	SiC MOSFET
Die size	1200 μm x 2200 μm
SiC-MOSFET	SiC MOSFET
Chip manufacturing process	SiC MOSFET
SiC-MOSFET	SiC MOSFET
Metal interconnect	Aluminum
Characteristic Feature	High voltage SiC MOSFET
Applications	Industrial, Power, Automotive

1-1. Summary of analysis results

Package appearance

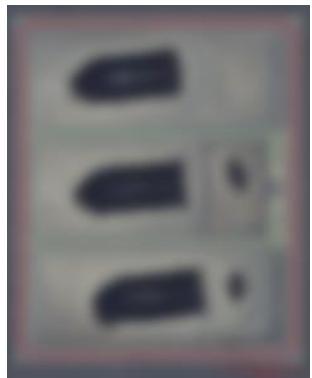


Cross-sectional structure analysis



SiC-MOSFET Die

Die size : [REDACTED] mm²



- planar-type gate, upper source metal 2-layer metal process
- The die edge withstand voltage structure uses a three-step JTE (Junction Termination Extension)

Die outer periphery



Source electrode

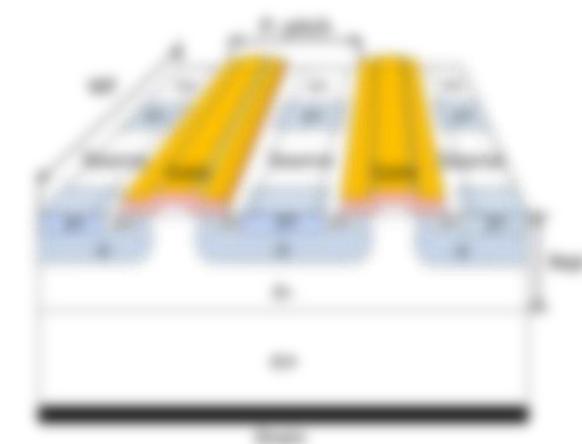
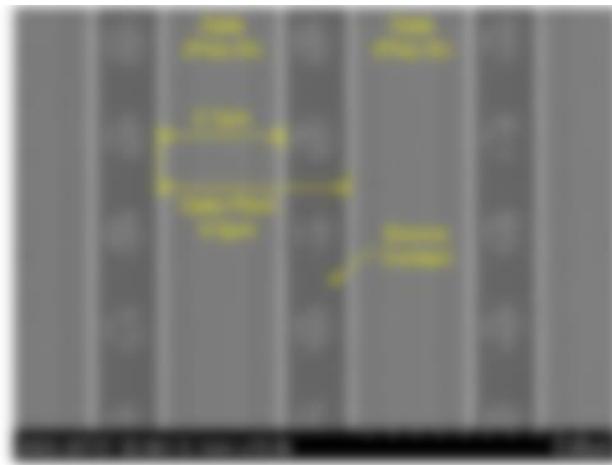


Table 2: Device structure SiC MOSFET

Region	Thickness	Material	Description
Gate	~100 nm	SiO ₂	Gate oxide
Drain contact	~100 nm	Al _x Si _y	Drain contact metal
Drain region	~100 nm	SiC	Drain region of the MOSFET
Drain p+ region (epitaxial)	~100 nm	SiC	Drain p+ region of the MOSFET (epitaxial layer)
Drain n+ region	~100 nm	SiC	Drain n+ region of the MOSFET
Source contact	~100 nm	Al _x Si _y	Source contact metal
Source region	~100 nm	SiC	Source region of the MOSFET
Source p+ region (epitaxial)	~100 nm	SiC	Source p+ region of the MOSFET (epitaxial layer)
Source n+ region	~100 nm	SiC	Source n+ region of the MOSFET
Gate metal	~100 nm	Al _x Si _y	Gate metal
Drain bus bar	~100 nm	Al _x Si _y	Drain bus bar
Source bus bar	~100 nm	Al _x Si _y	Source bus bar
Drain interconnect	~100 nm	Al _x Si _y	Drain interconnect
Source interconnect	~100 nm	Al _x Si _y	Source interconnect

Table1-3: Device structure: Layers material and thickness

Layer description	Thickness	Material	Properties
Wafer type•configuration (Bulk, Epi)	~1000µm	Si	Carrier concentration 8.407 Pg, 8.000 Sheet resistance 10.000 Ohm/square
N-epi layer	~1µm	Si	Carrier concentration 8.000 Pg, 8.000 Sheet resistance 10.000 Ohm/square
N Buffer layer	~0.0015µm	Si	Carrier concentration 8.000 Pg, 8.000 Sheet resistance 10.000 Ohm/square
Pwell implant depth	~1.5µm	Si	Carrier concentration 1.00 Pg, 1.000 Carrier region carrier concentration 1.0 - 10 ¹⁷ cm ⁻³ , 10.000 Pg, 4.000
N+ implant depth	~0.0005µm	Si	Carrier concentration 4.2 - 10 ¹⁷ cm ⁻³ , 10.000 Pg, 4.000
Gate electrode structure/material	~0.5µm	TiAl ₅ / Ti	TiAl ₅ Pg, 1.0-10
Gate dielectric layer	~0.0005µm	SiO ₂ / Si ₃ N ₄	TiO ₂ Pg, 1.0-10
Field oxide layer	~0.5µm	SiO ₂	TiO ₂ Pg, 1.0-10, TiO ₂ Pg, 1.0-10
Silicide layer	~0.0005µm	Si	TiO ₂ Pg, 1.0-10
Source barrier layer (M1)	~0.0005-0.001µm	Ti _x N _y	TiO ₂ Pg, 1.0-10, TiO ₂ Pg, 1.0-10
Source metal M1	~0.0005µm	Al/Ni/Au	Al Pg, 10-100
Source barrier layer (M2)	~0.0005µm	Ti _x N _y	TiO ₂ Pg, 1.0-10
Source metal M2	~0.0005µm	Al/Ni/Au	TiO ₂ Pg, 1.0-10
ILD1 (Between gate and M1)	~0.01-0.05µm	SiO ₂ / Si ₃ N ₄	TiO ₂ Pg, 1.0-10, TiO ₂ Pg, 1.0-10
ILD2 (Between M1-M2)	~0.01-0.05µm	SiO ₂	TiO ₂ Pg, 1.0-10
Protection layer	~0.001-0.005µm		
Die back-side metal	~0.0005-0.001µm	Ti _x N _y	TiO ₂ Pg, 1.0-10. Description in the order in which they are formed from the back side.

2. Package Analysis

2-1. Appearance observation

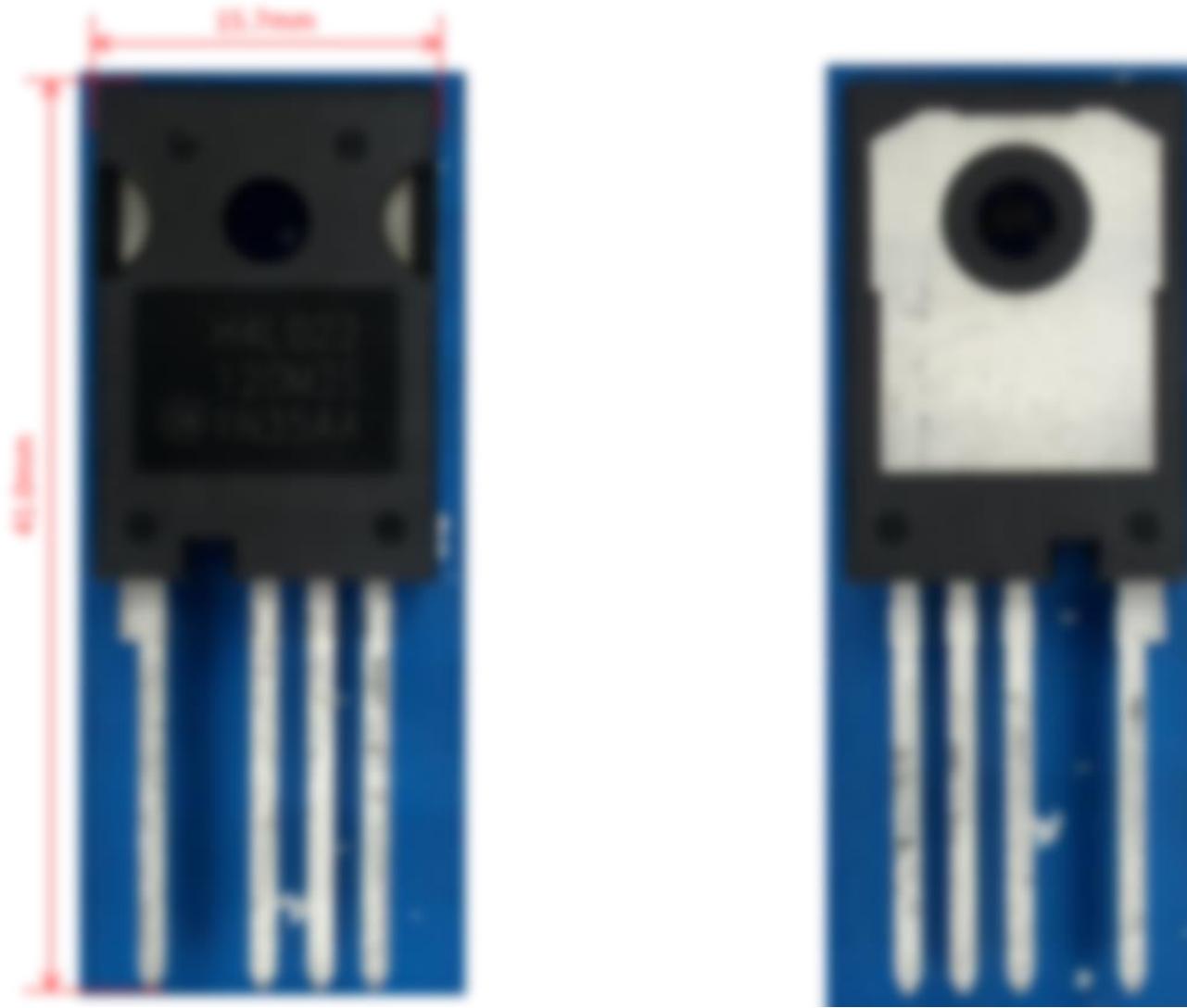


Fig. 2-1-1 Package observation

2-1. Appearance observation

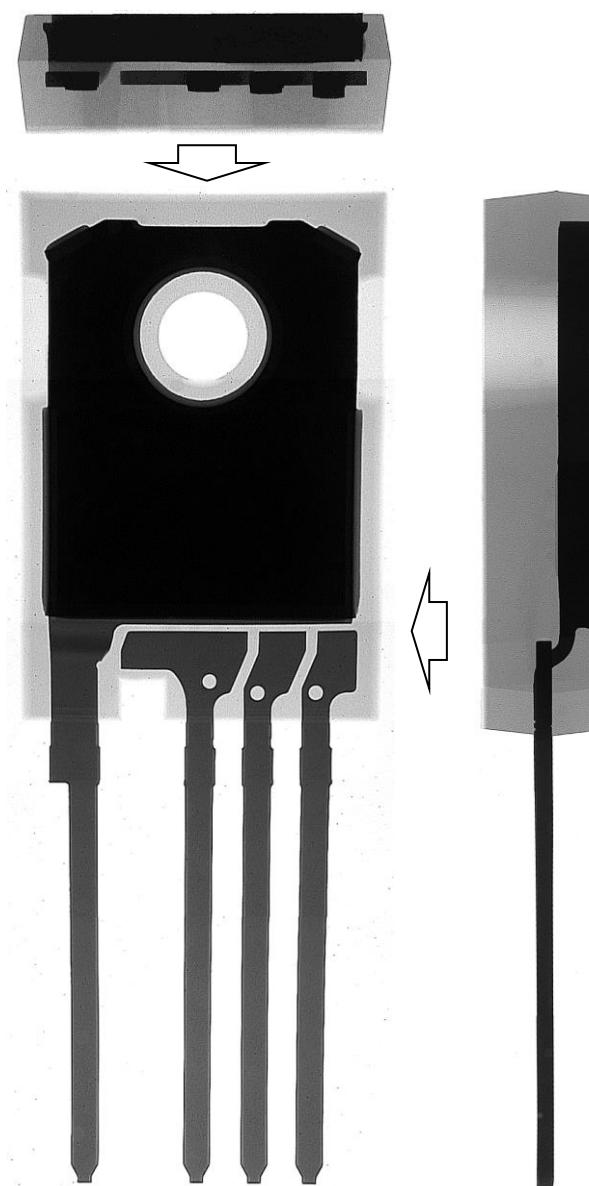


Fig. 2-1-2 X-ray image (front/side)

2-1. Appearance observation

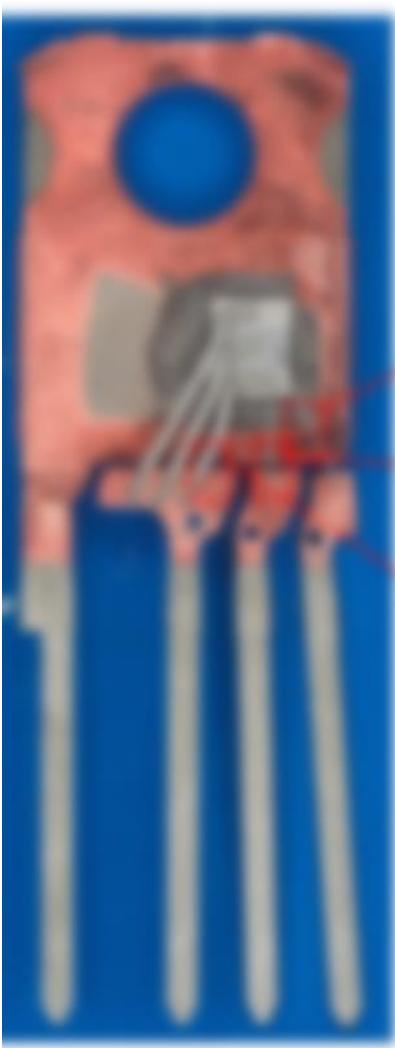


Fig. 2-1-3 Internal layout observation

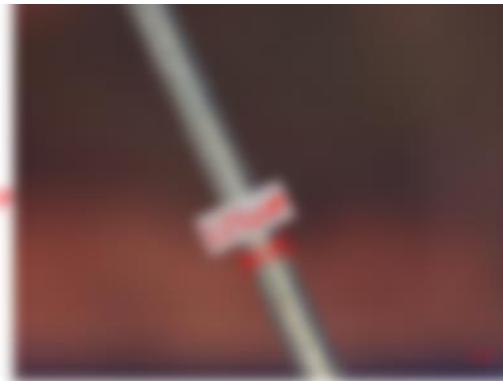


Fig. 2-1-4 Source/drain wire



Fig. 2-1-5 Source/drain wire



Fig. 2-1-6 Source/drain wire

2-2. Die Observation

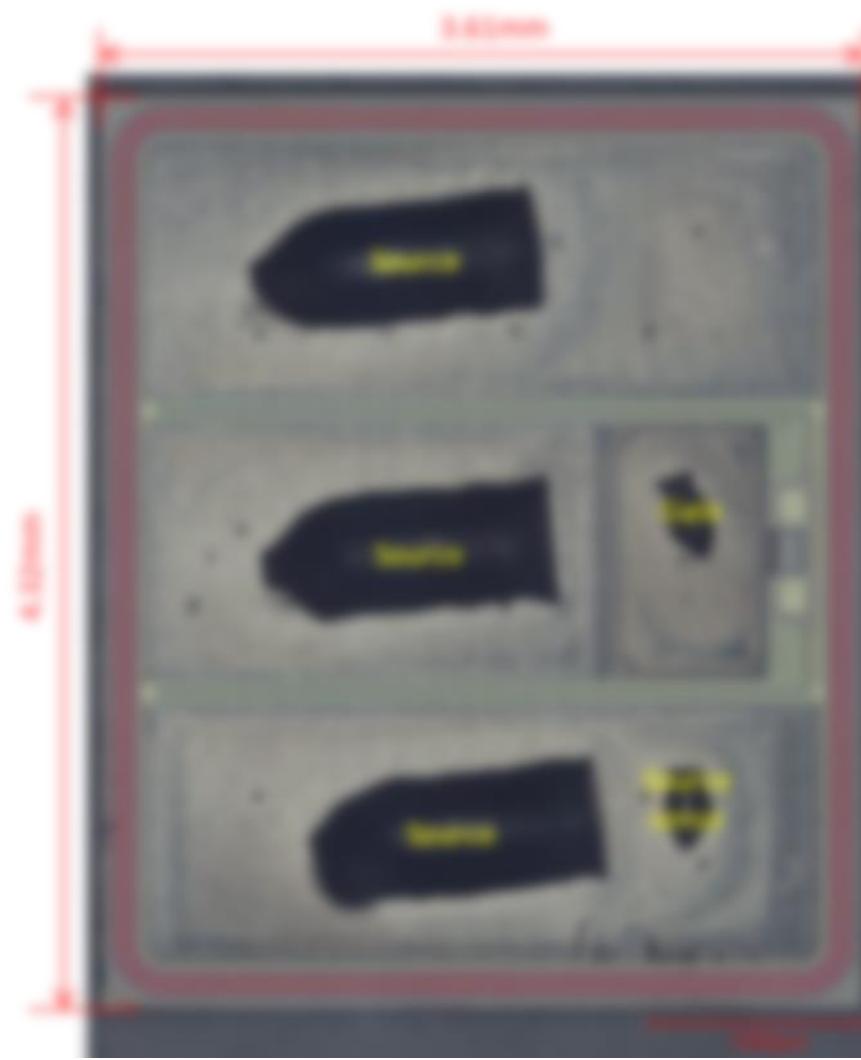


Fig. 2-2-1 Die picture (Top Metal layer)

3. SiC MOSFET structure analysis

3-1. Plane structure analysis by Optical Microscope

Die size
Active area

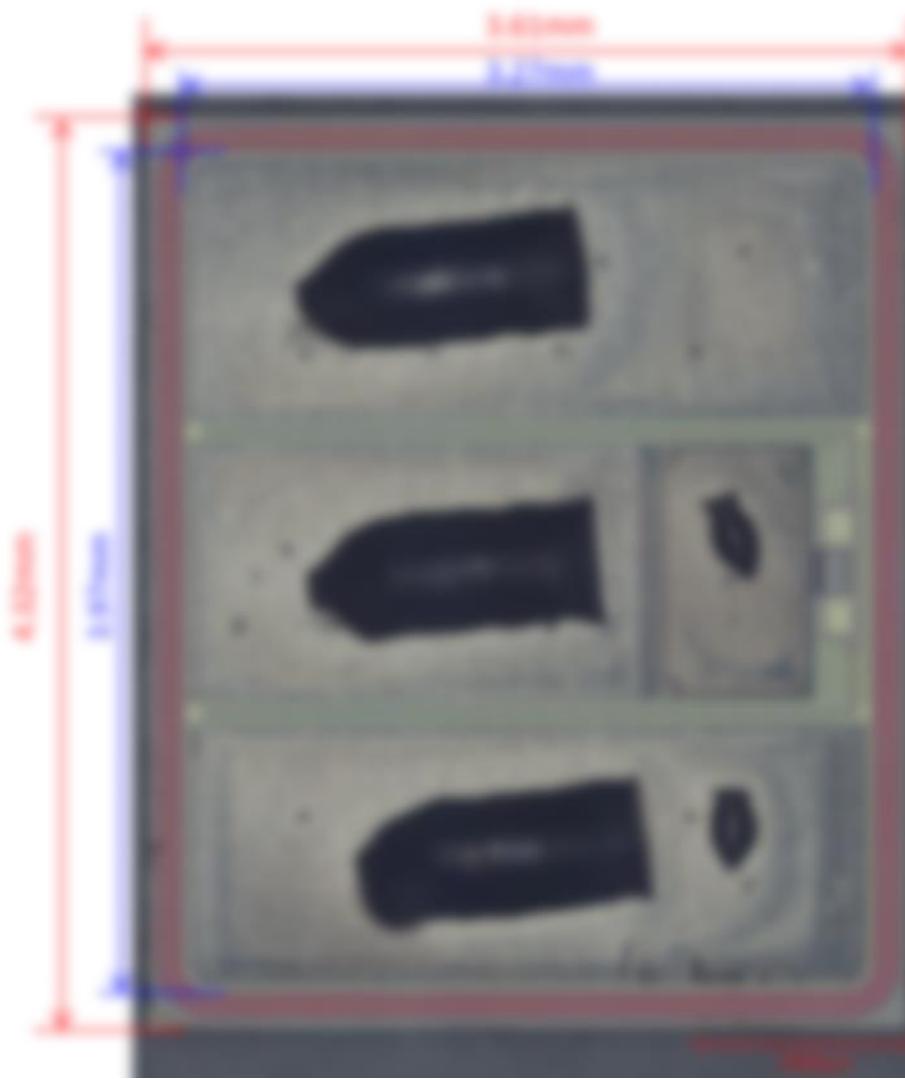


Fig. 3-1-1 Die photo (Top Metal layer)

3-1. Plane structure analysis by Optical Microscope

※ In this chip layout the gate resistor is shorted by M1.



Fig. 3-1-4 Gate electrode pad (Top Metal layer)

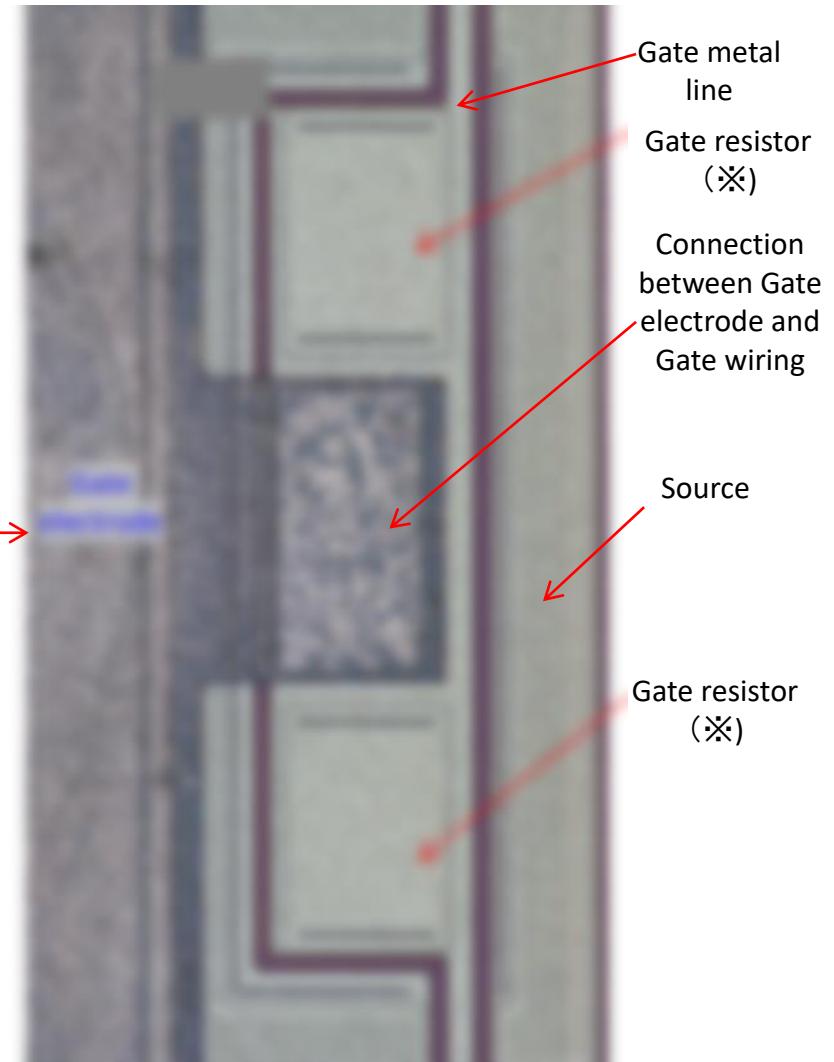
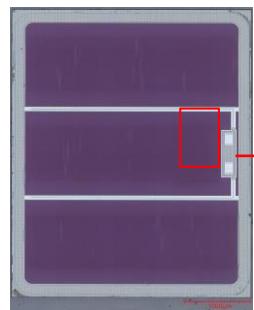


Fig. 3-1-5 Gate electrode pad (Top Metal layer)

3-1. Plane structure analysis by Optical Microscope



【Poly-Si layer (Top Metal removed)】

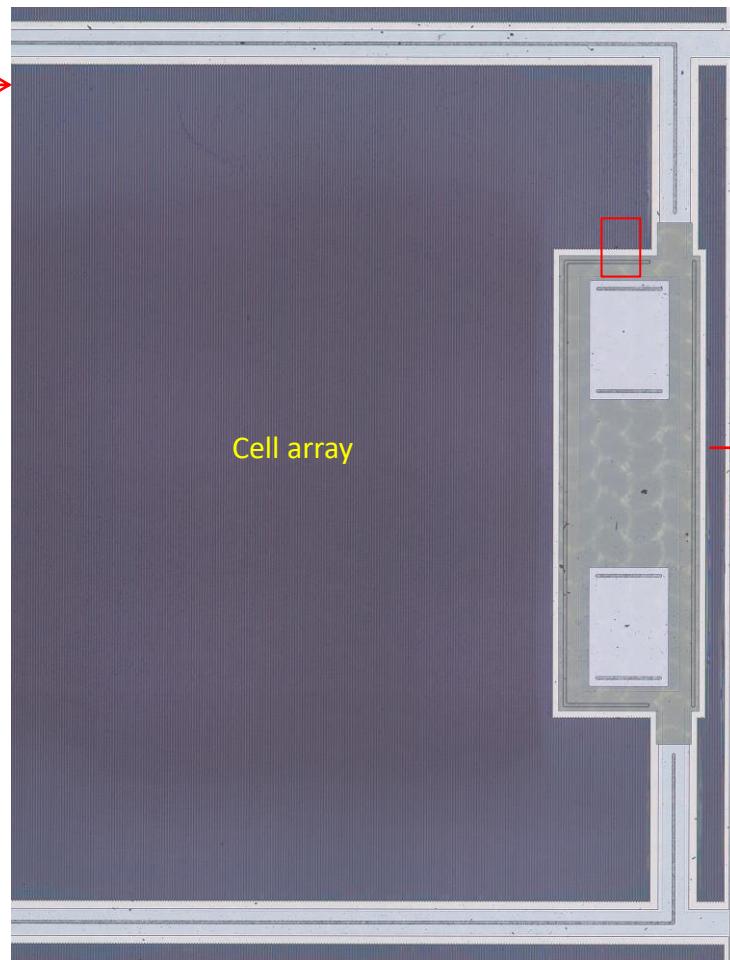


Fig. 3-1-17 Gate Pad area (Poly-Si layer)

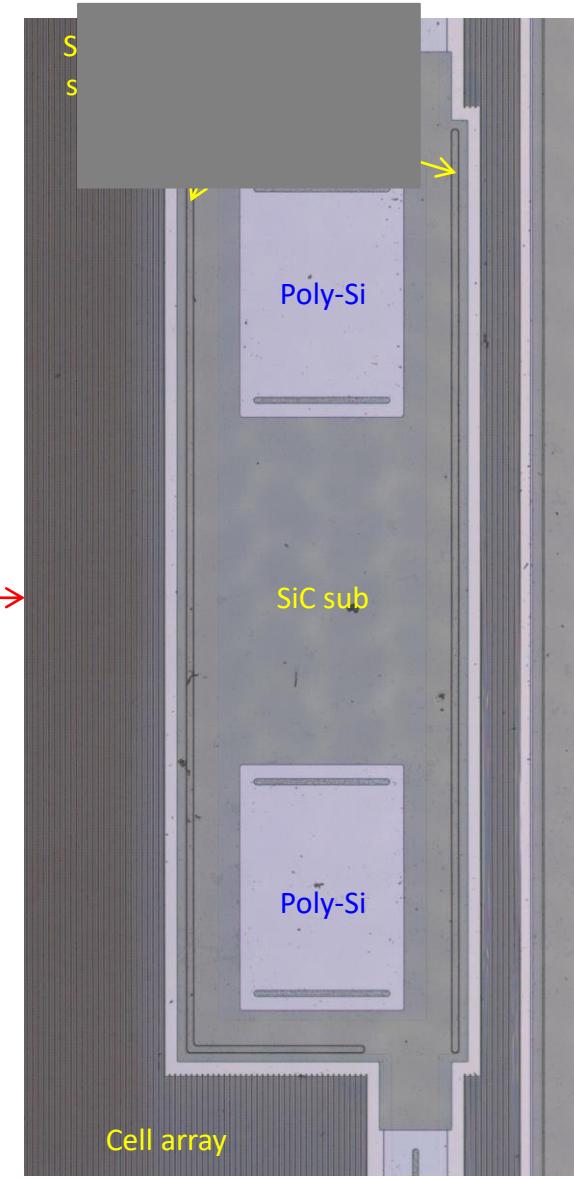


Fig. 3-1-18 Gate Pad Gate resistor (Poly-Si layer)

3-2. Plane structure analysis by SEM

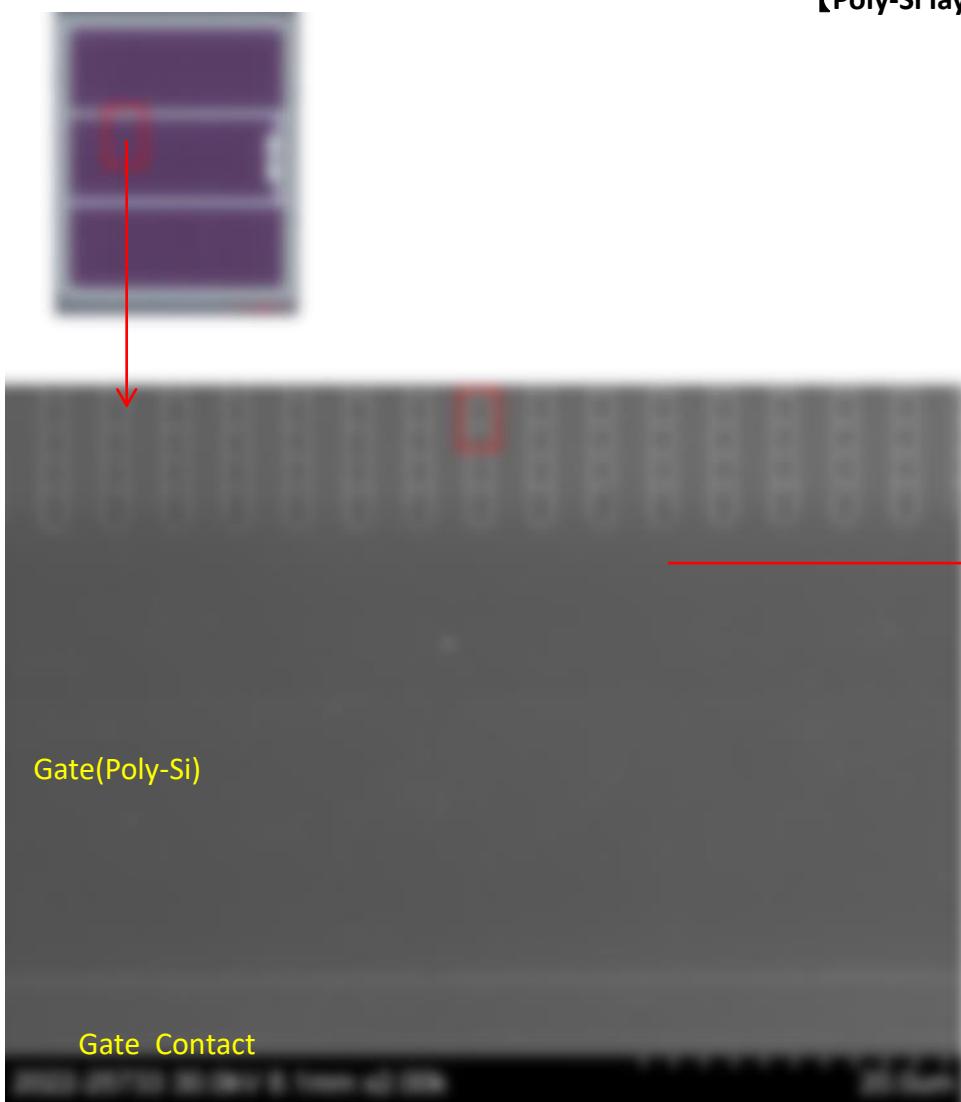


Fig. 3-2-5 Cell area edge plane SEM image (Poly-Si layer)

【Poly-Si layer (Top Metal removed)】

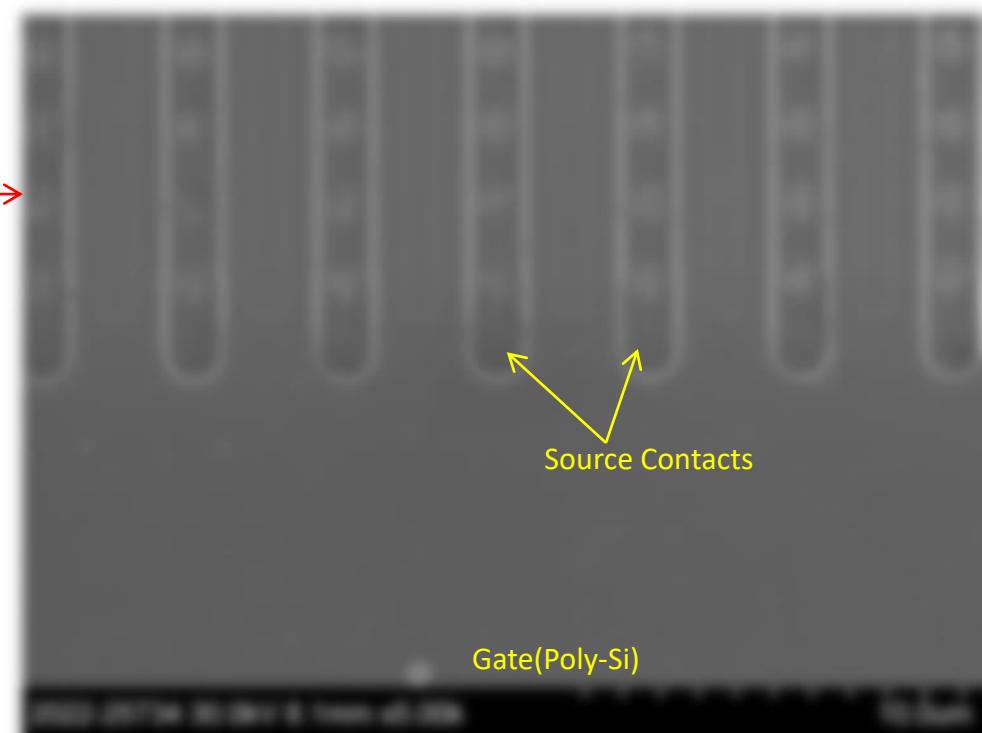


Fig. 3-2-6 Cell area edge plane SEM image (Poly-Si layer)

3-2. Plane structure analysis by SEM

【SiC substrate layer (Poly-Si, isolation films removed)】

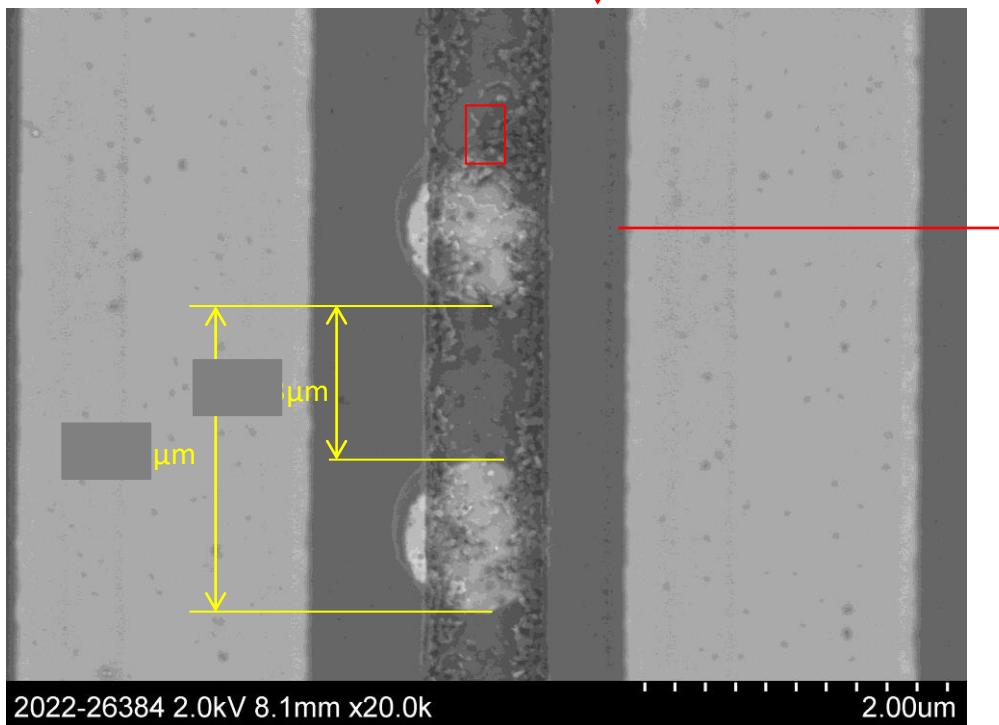


Fig. 3-2-18 Cell area plane SEM image (SiC substrate layer)

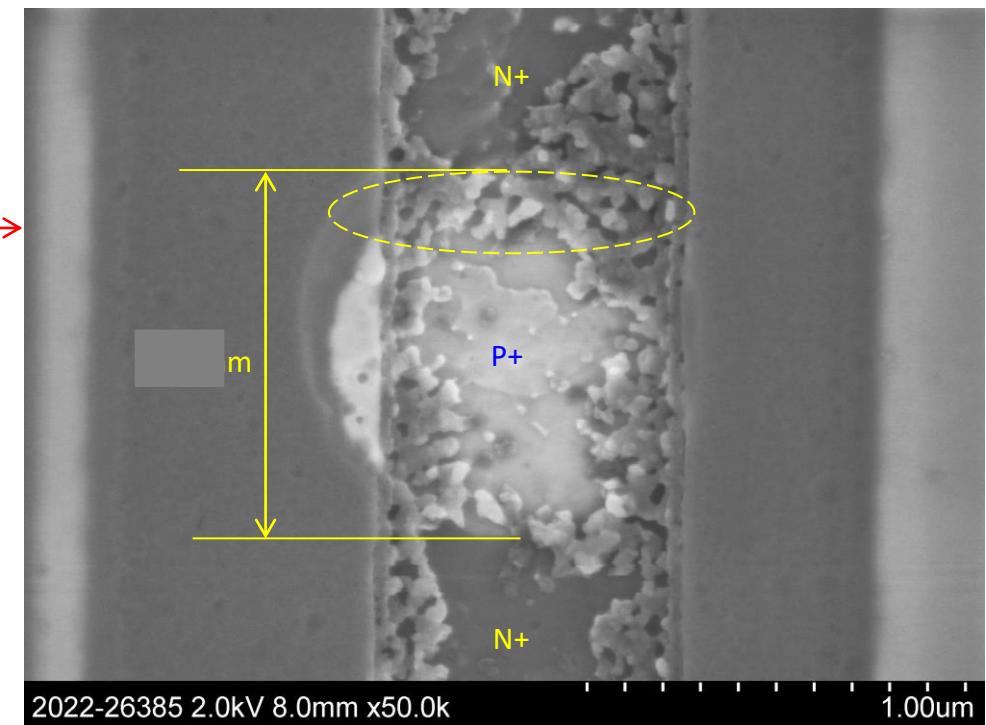


Fig. 3-2-19 Cell area plane SEM image (SiC substrate layer)

3-3. Cell area cross-sectional structure analysis

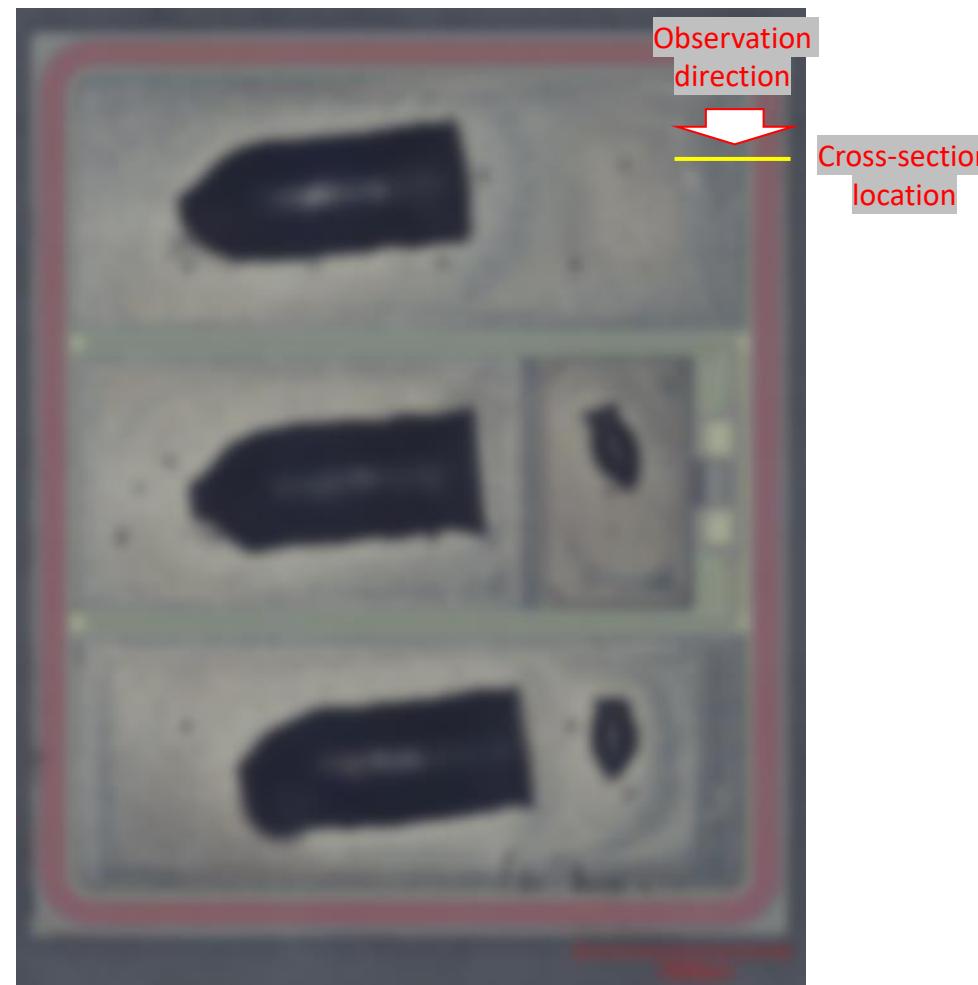


Fig. 3-3-1 Die image (Top Metal layer)

3-3. Cell area cross-sectional structure analysis

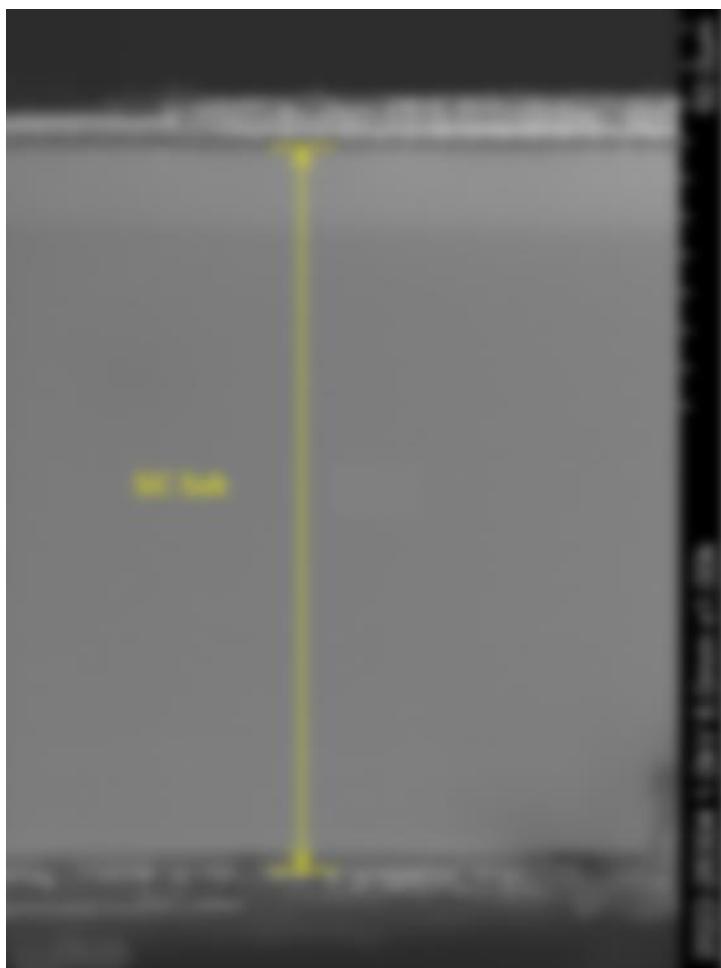


Fig. 3-3-2 Die cross-section SEM image

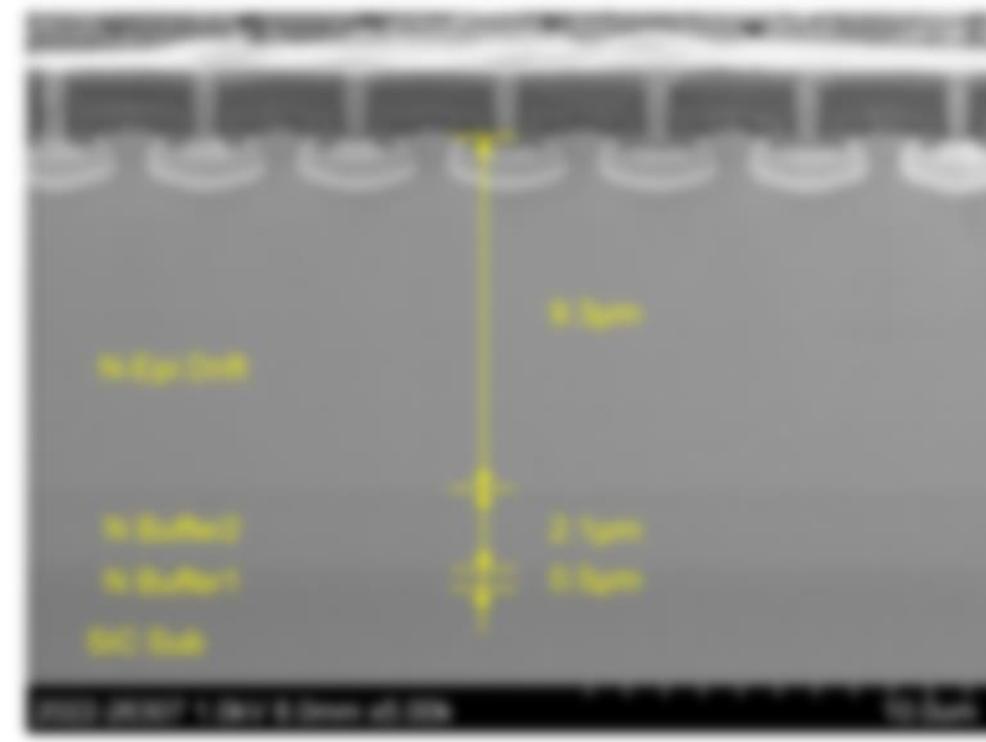


Fig. 3-3-3 N-Epi layer SEM image

3-3. Cell area cross-sectional structure analysis

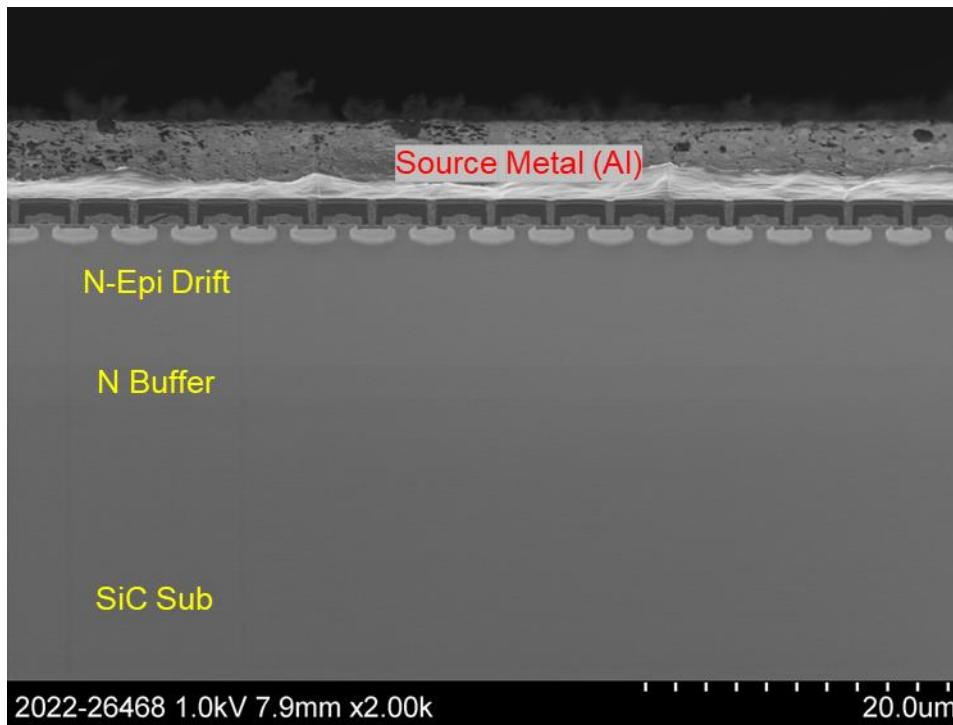


Fig. 3-3-4 Cell area cross-sectional SEM image

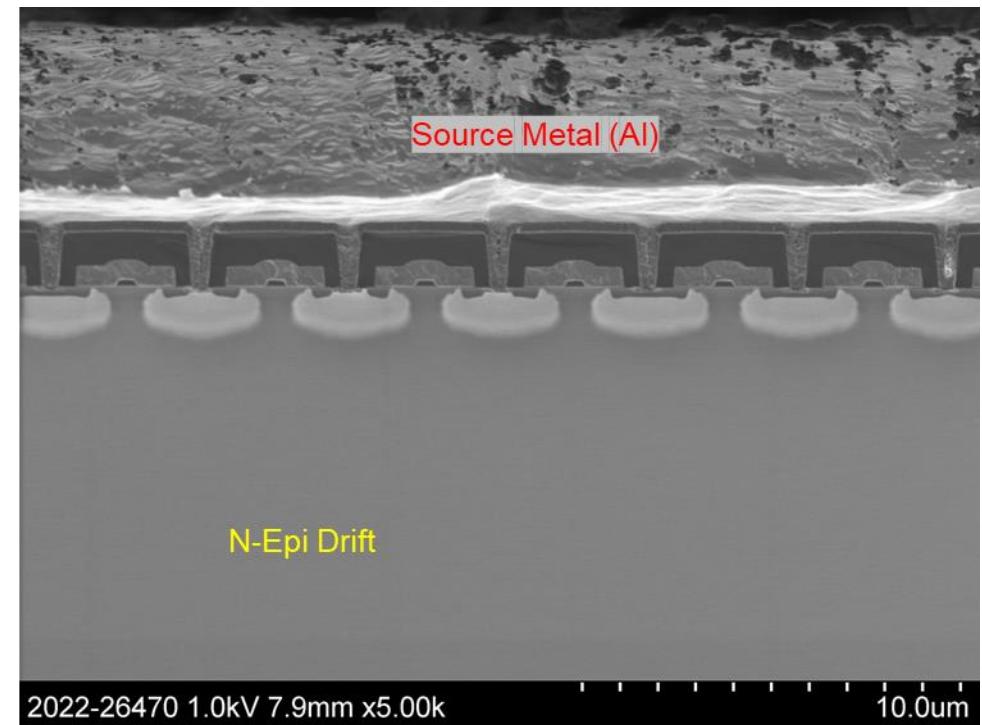


Fig. 3-3-5 Cell area cross-sectional SEM image

※ Implanted layer estimate

3-3. Cell area cross-sectional structure analysis

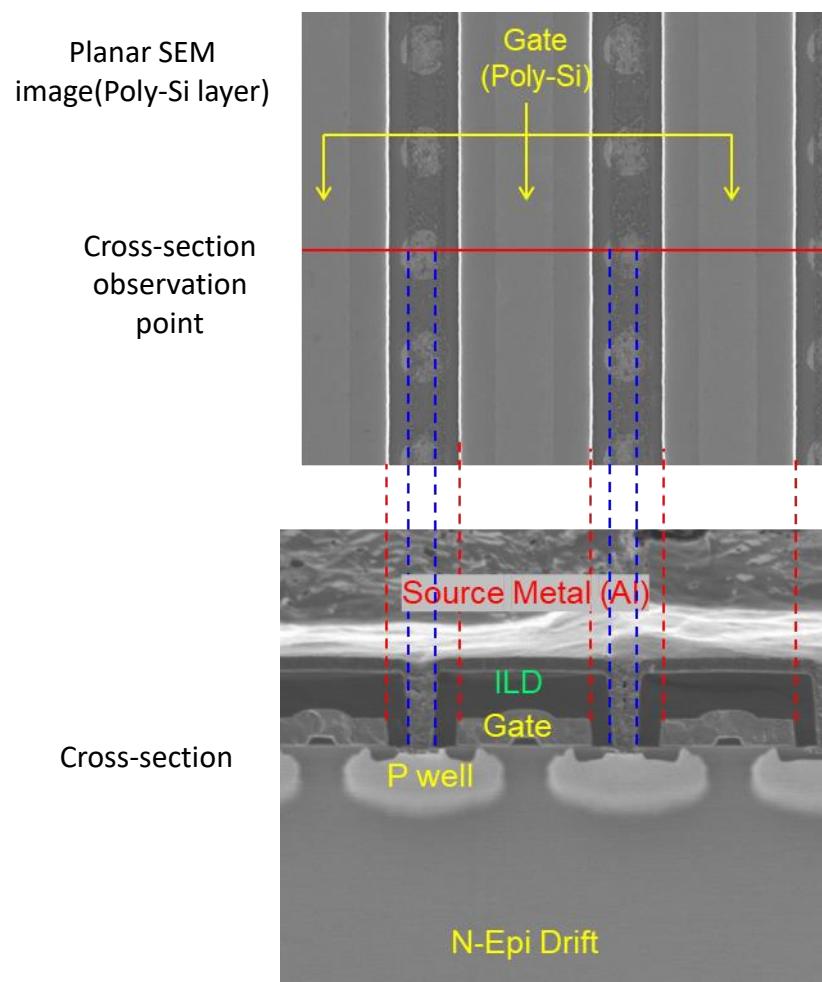


Fig. 3-3-6 Cell area SEM image

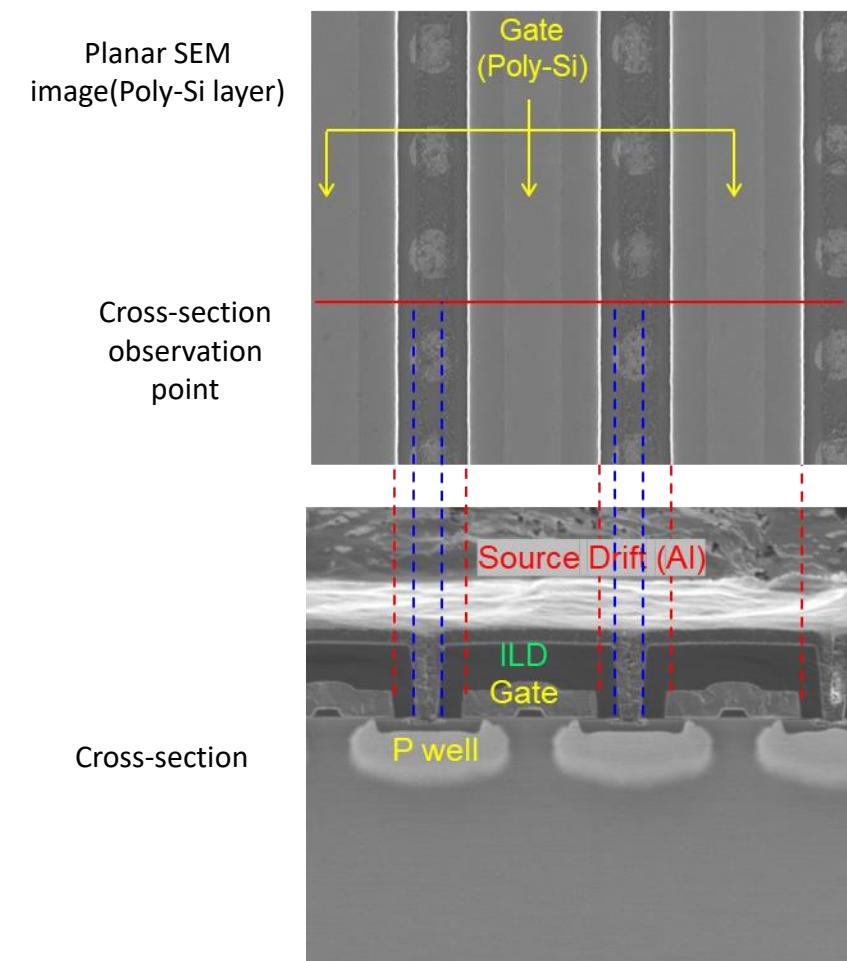


Fig. 3-3-7 Cell area SEM image

3-3. Cell area cross-sectional structure analysis

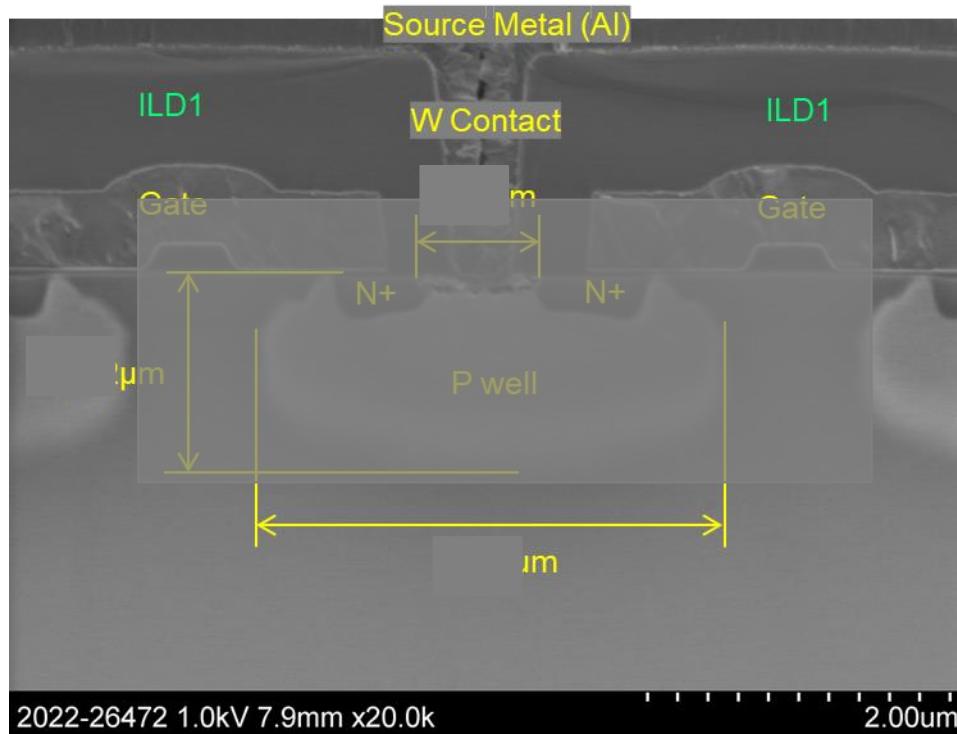


Fig. 3-3-10 Cell area SEM image

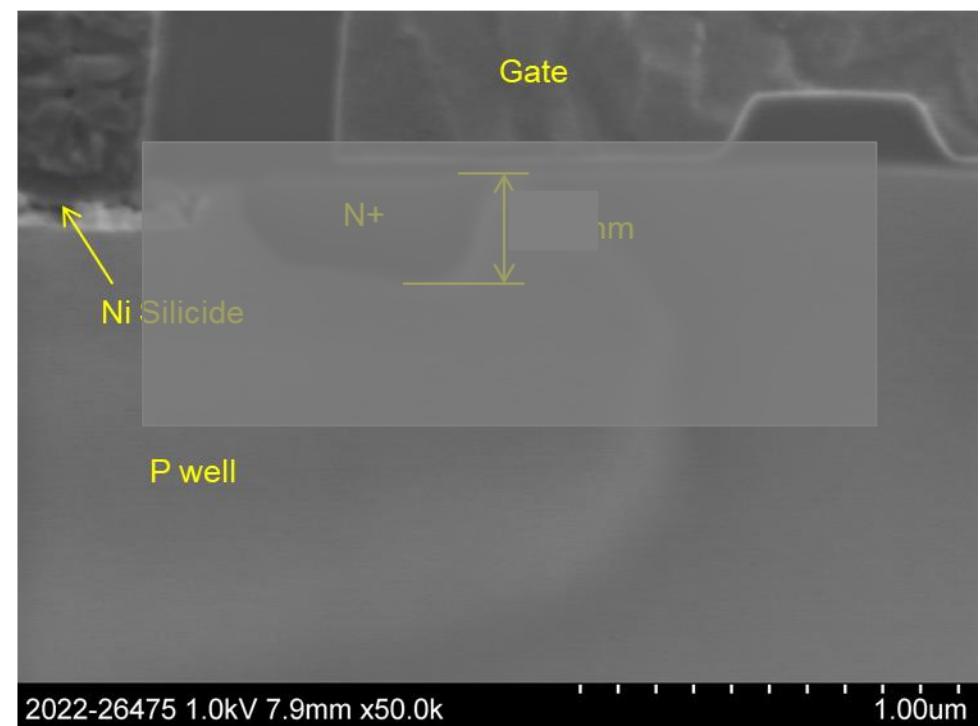


Fig. 3-3-11 Cell area SEM image

3-3. Cell area cross-sectional structure analysis

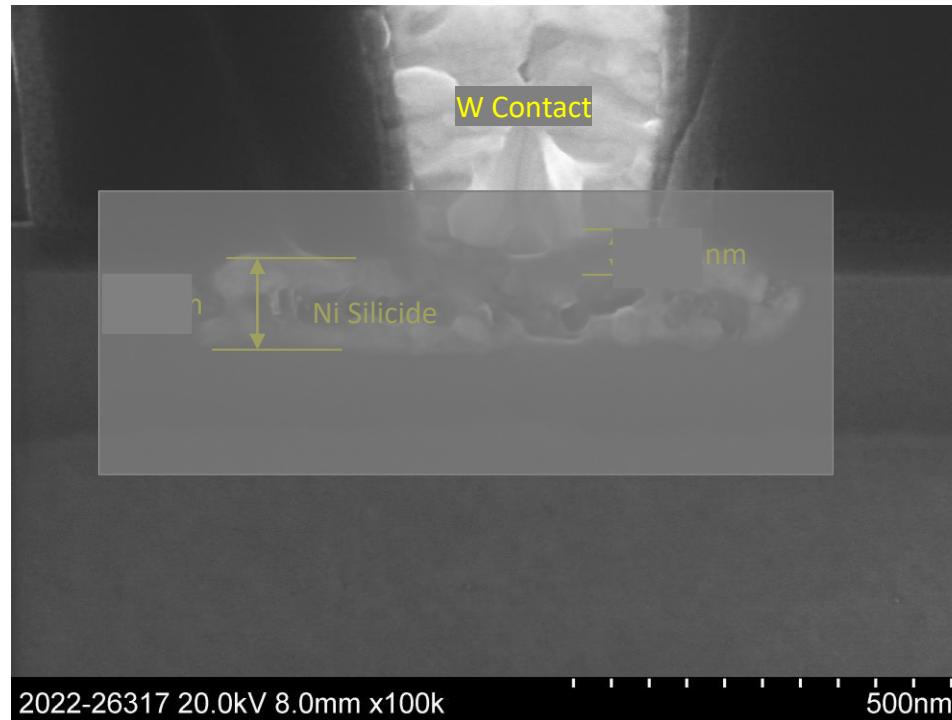


Fig. 3-3-17 Cell area SEM image

3-5. MOSFET gate pad cross-sectional structure analysis

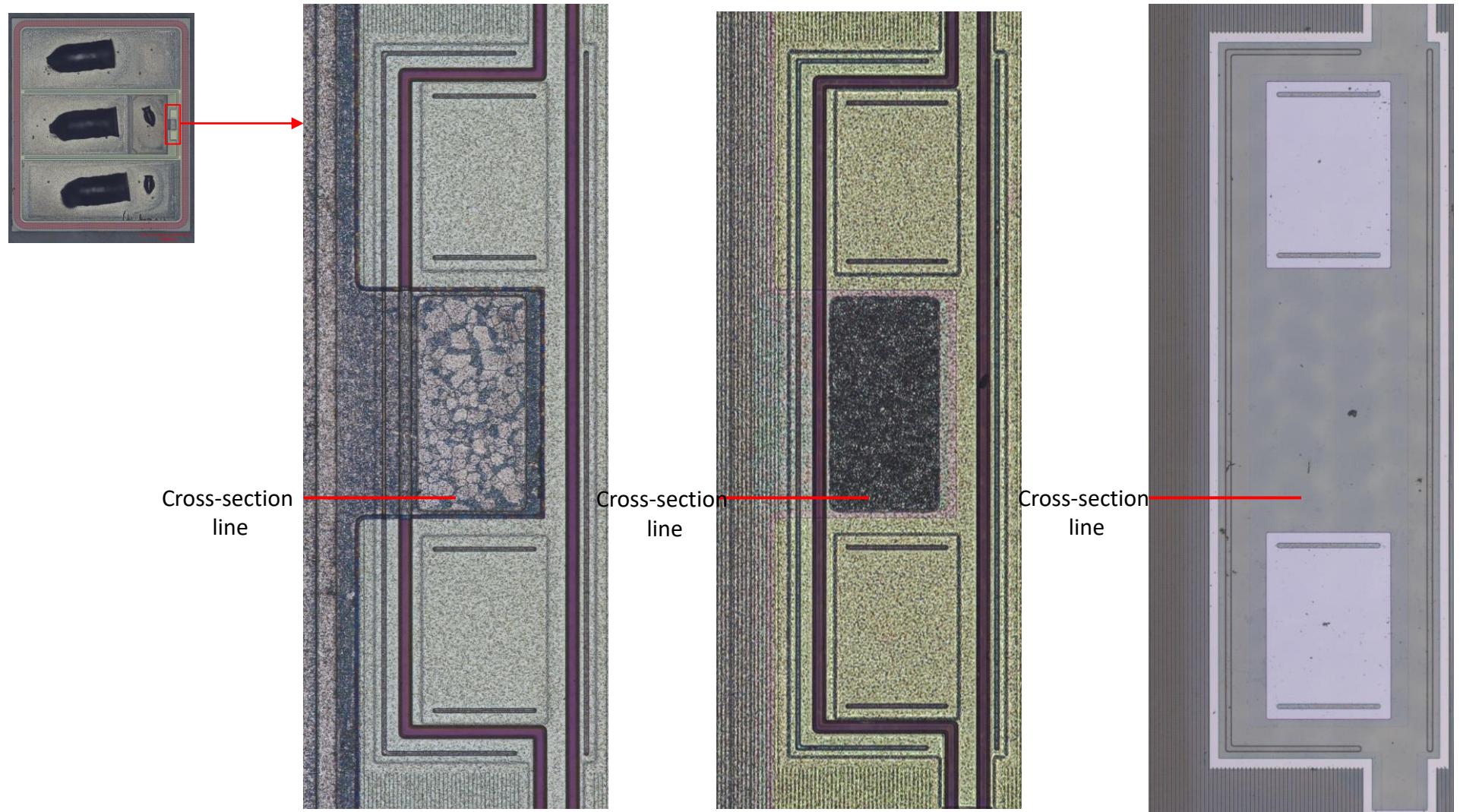


Fig. 3-5-1 Gate Pad cross-section processing location

4. SCM / SMM Analysis

4-1. SCM / SMM Analysis Results

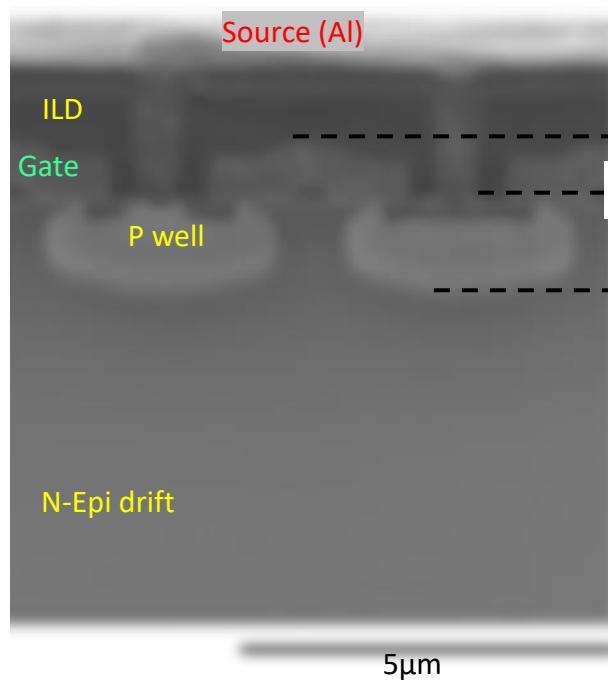


Fig. 4-1-1 Cell area cross-sectional SEM.

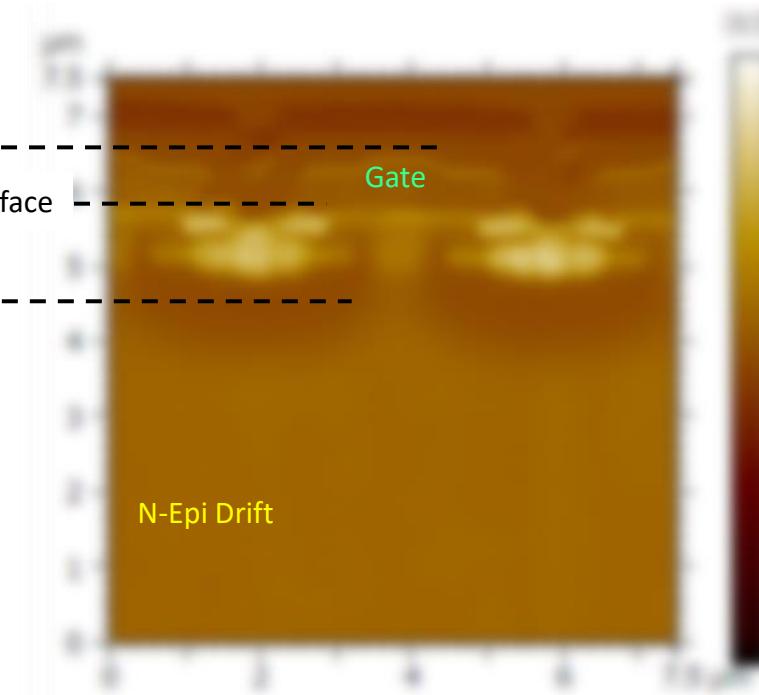


Fig. 4-1-2 Cell area cross-sectional AFM.

4-1. SCM / SMM Analysis Results

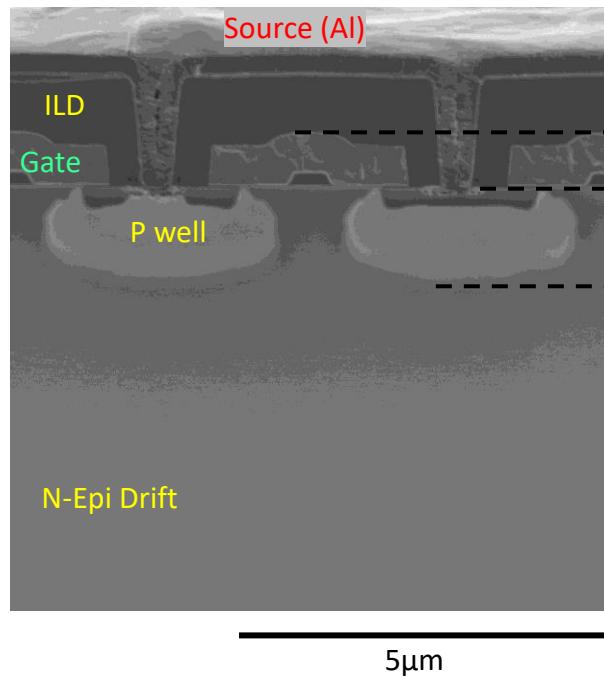


Fig. 4-1-5 Cell area cross-sectional SEM.

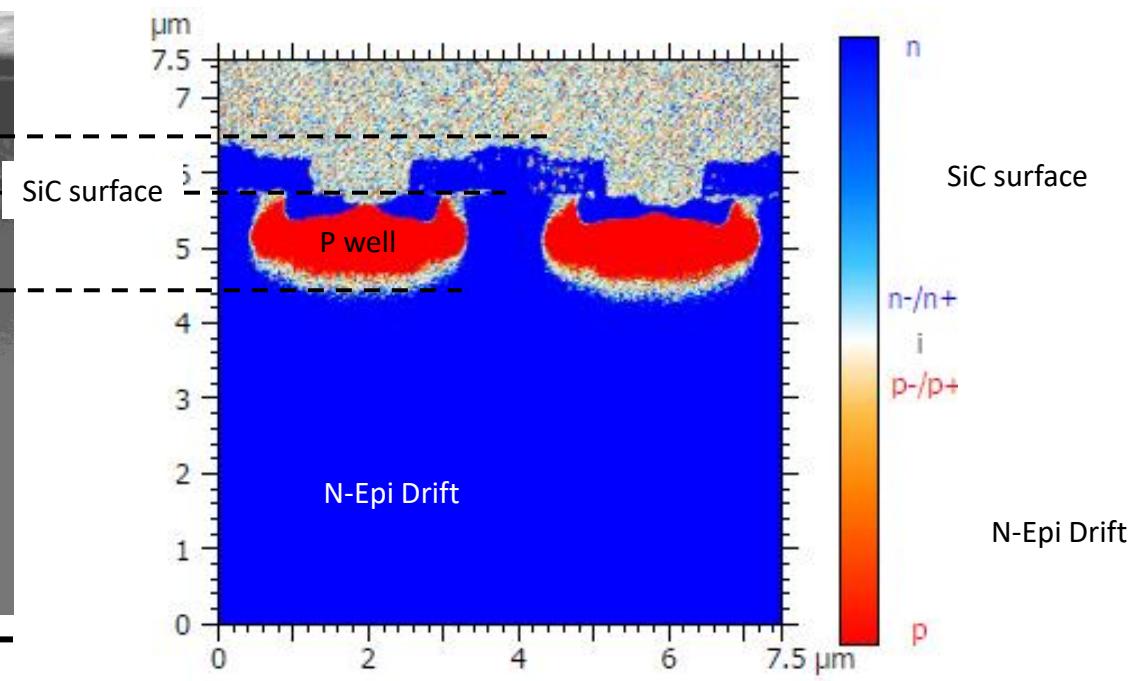


Fig. 4-1-6 Cell area SCM image (scale enhancement)

4-1. SCM / SMM Analysis Results

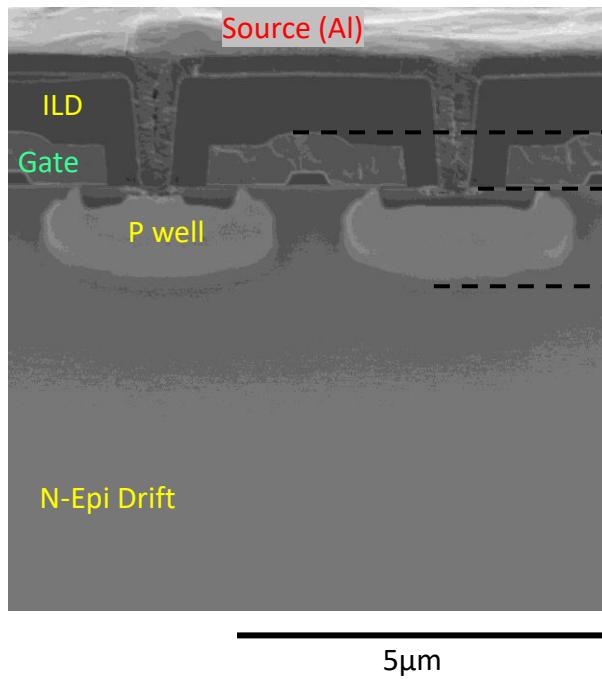


Fig. 4-1-7 Cell area cross-sectional SEM.

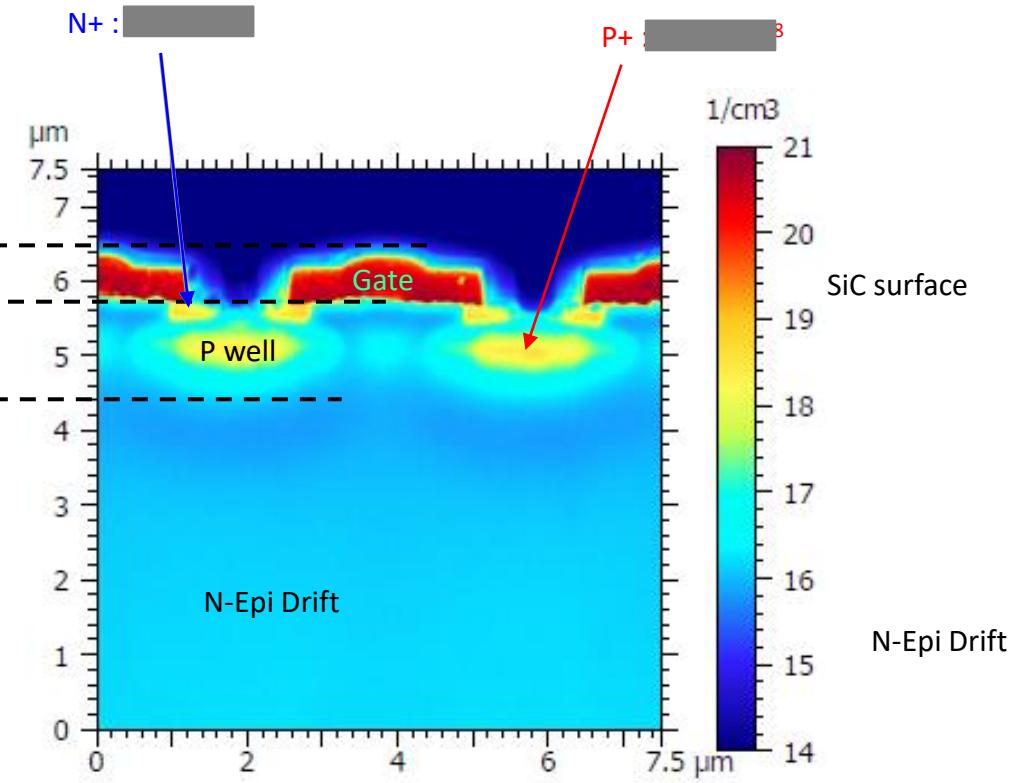


Fig. 4-1-8 Cell area SMM carrier concentration conversion image

4-2. SCM / SMM Line Analysis

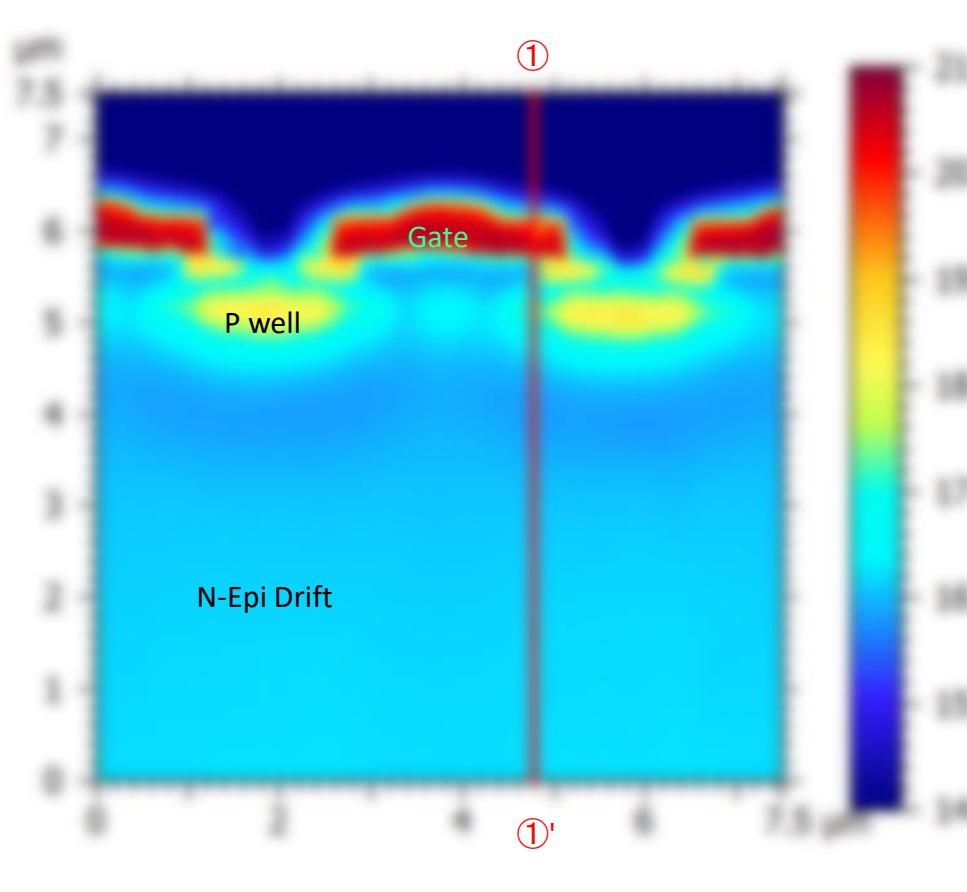


Fig. 4-2-1 Cell area SMM carrier concentration conversion image

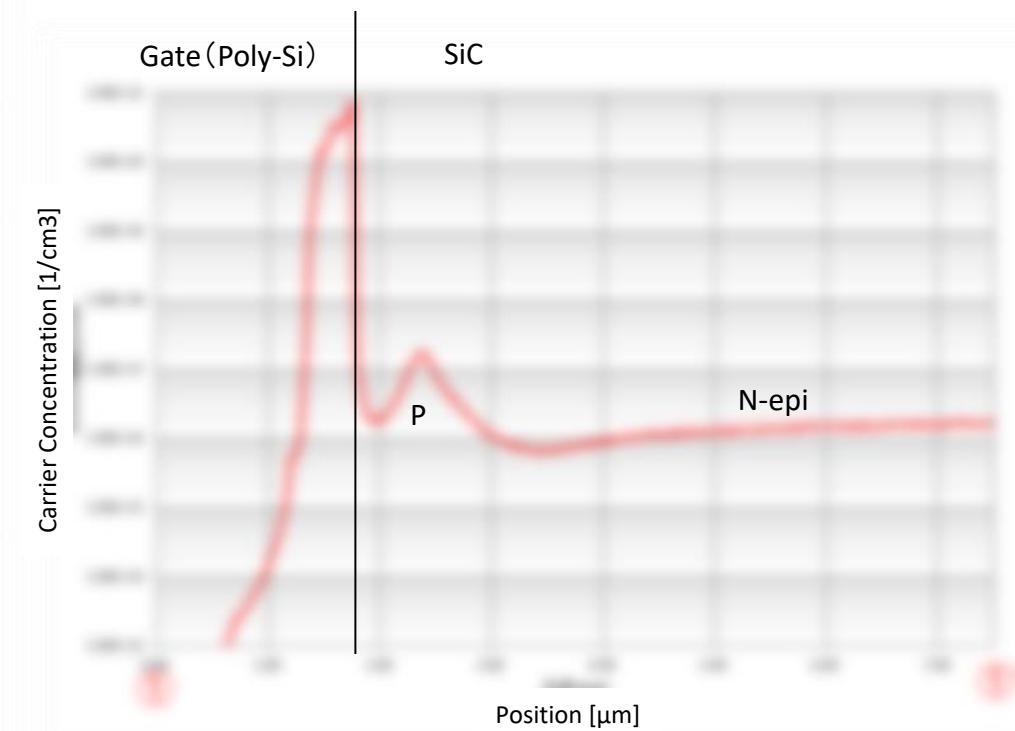


Fig. 4-2-2 Line doping profile ①