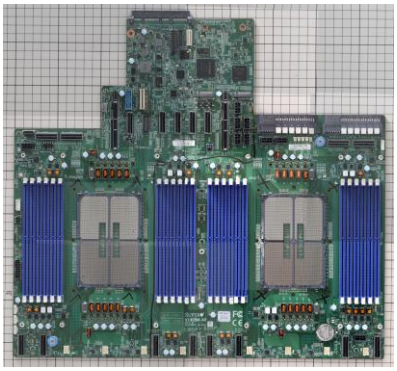
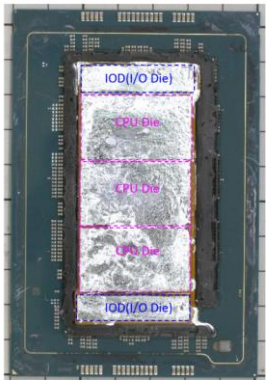
Server: Intel Xeon 6980P-equipped Supermicro Server PCB and Package Analysis Report (Announcement)

Supermicro: 2U Hyper SuperServer (SYS-222HA-TN)



Main PCB

Package



Removed of heat sink

Product Overview

Servers equipped with the Intel Xeon 6980P provide an ultra-high-performance platform designed for next-generation data centers, supporting extremely demanding workloads such as AI inference and training, large-scale data processing, and HPC applications. The Xeon 6980P integrates 128 cores and 256 threads and is part of the latest Xeon 6 family built on the Granite Rapids-AP architecture, delivering both high power efficiency and computational performance through a 5 nm-class manufacturing process. It operates at a base frequency of 2.0 GHz and boosts up to 3.9 GHz, while its massive 504 MB L3 cache provides strong support for memory-intensive workloads. The processor also supports DDR5 MRDIMM (up to 8800 MT/s), achieving a memory bandwidth of up to 614 GB/s, which significantly enhances large-dataset processing capability. With PCIe 5.0 support, it ensures robust connectivity to high-speed accelerators and next-generation storage devices. The package integrates three CPU dies and two I/O dies, interconnected via EMIB.

EMIB: Embedded Multi-die Interconnect Bridge

This time, LTEC is going to release the following five reports:

- Investigation of semiconductor components mounted on the PCB 25R-1057-1
- Cross-section analysis of the board and package 25R-1057-2
- L/W measurement of the finest features across 20 board layers 25R-1057-3
- L/W measurement of the finest features across 18 package layers 25R-1057-4
- L/W measurement of the finest features across 5 EMIB layers 25R-1057-5
- Analysis of CPU and IOD chips (Cross-section and Floor plan analysis 25R-1057-6

Details will be provided on the next page.

Report No.: 25R-10571,2,3,4,5,6 Release : 2026/ 4

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Report

1. Report (1) : Survey of Key Semiconductor and Components mounted on the PCB

Scheduled Release: November 30
- Survey of mounted semiconductor devices
- Datasheets (if available)
- Enlarged photographs of mounted components such as sockets

2. Report (2) : Cross-section Analysis of PCB and Package

Scheduled Release: November 30
- X-ray images of the package
- Cross-section structural analysis
- Measurement of individual layer thicknesses

3. Report (3) : L/W Measurement of the Finest Features Across each 14 PCB Layers

Scheduled Release: December 19
- Measurement of line width and line pitch of the finest features in each of the 14 layers

4. Report (4) : Image Data of 20 Package Layers

Scheduled Release: November 30
- Wiring information (photographs of each of the 20 layers, line width, line pitch)
- Optional: CAD data (ODB++ etc.) available (additional fee is required)

5. Report (5) : Analysis of CCD and IOD Dies

Scheduled Release: January 30, 2026
SEM cross-section of Seal Ring area
Photographs of top layer and gate layer
Optional: Functional estimation available (additional fee is required)

For inquiries regarding report pricing, please feel free to contact LTEC.

Report No : 25R-0714-1,2,3,4,5 Release day :

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